Book 3 of 3

500-ME-12257

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MANUAL ADDENDUM

for

MODEL 3440

P/N 356-0205-504, 505

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Section 1
GENERAL DESCRIPTION

1.0 INTRODUCTION

This manual contains information regarding the Model DAC021 Digital to Analog Converter module and the Model CPI012 Computer Interface module as provided in the Model 3440 Format Synchronizer. Section 1 provides general information about the two modules. Section 2 provides the input/output pin connections (at the rear panel of the Model 3440) while section 3 deals with programming and setup of these two modules. Section 4 provides the theory of operation and section 5 contains each module's parts list and schematics.

1.1 PURPOSE OF EQUIPMENT

The CPI012 module provides the interface between the format synchronizer's output and the input to a DEC computer. The CPI012 supplies data to either of two DRB32W interfaces. Only one of these two interfaces can be active at any one time.

The DAC021 converts digital data words into equivalent analog values. The DAC021 provides 16 D/A's that can be programmed to convert any 16 parameters in a PCM data stream. The DAC021 also provides 3, 16 bit event registers that can store any 3 parameters from the input stream. The outputs from the event registers are not available on the current unit only the 16 D/A's are brought out to the unit's rear panel.

1.2 PHYSICAL DESCRIPTION

The two modules are each contained on a triple Eurocard outline, measuring 11 inches by 14 inches with 3, 96 pin DIN connectors. The DAC021 module is mounted in card slot 5 and the CPI012 is mounted in slot 7. The outputs from these modules are routed to the rear panel where the DAC021's signals are on J15 and the CPI012's outputs are on J11 and J12 for interface number one and J13 and J14 for interface number 2.

1.3 FUNCTIONAL DESCRIPTION

1.3.1 DAC021

Figure 1-1 is a block diagram of the DAC021 module. The circuitry consists of two functional paths, one relative to the data and the other to the generation of a strobe for storing the appropriate data in the DACS and DERS. The top half of the block diagram relates to the strobe generation while the bottom half addresses data manipulation.

The generation of a strobe at the proper time is accomplished by storing in RAM, a marker that identifies those word(s) selected for distribution to the DACS and DERS. The marker consist of the DAC number represented by a 5 bit binary code (DAC's from 1 to 16 and the DER's from 17 through 19). The binary code is written into the RAM during setup at locations that correspond to the selected word/frame number where they occur in the PCM format. The RAM is then addressed by the word and frame count outputs from the frame sync and when there is a correspondence between the address and the word/frame counts, a equivalent DAC/DER binary number is output and decoded to produce a strobe.

In the block diagram, the word count is stored in a register whose output is applied to the address lines of the 65K x 8 bit WORD RAM. The lower 5 bits (0 to 4) of the RAM define the address of the DAC or DER that is to be loaded with the data from the frame sync. Bit 7 of the WORD RAM selects which RAM (WORD or FRAME) is to be used. The WORD RAM is used to define minor frame words and the FRAME RAM is used to define major frame words (subcommutated words). For subframe words, the output of the WORD RAM (bits 0 to 3) is used to control the upper 4 bits of the FRAME RAM address lines. The selected RAM output is

applied to a 5 bit binary decoder that determines which one of the DAC's or DER's will be strobed. A binary output of zero is used to signify that no DAC or DER has been selected. The real-time strobe is generated by passing the end of word strobe +1 through a delay circuit to compensate for the delay encountered by the data in the data path.

The 19 lines decoded from the RAM binary output is sent to a 2 to 1 multiplexer that selects between real-time and calibration strobes. The calibration strobe is generated when a write strobe is generated for register 1. The strobe is passed through a delay to permit the calibration data to stabilize.

The data path begins with the storing of the frame sync parallel output by a register. The output from the register is sent to a shifter circuit that aligns the input data such that the MSB of the input data path lines up with the MSB of the DAC input (DAC input is 12 bits whereas the frame sync input can be from 6 to 16 bits). The shifter circuit is active only for data that is LSB justified. When frame sync data has been MSB justified, it is flipped at the input to the justification multiplexer. The justification multiplexer selects between LSB and MSB justified data. The output of this mux is buffered, inverted and sent to the DAC's. Calibration data is buffered and tied to the DAC's also, but will only be active in the CALIBRATION mode.

Data for the DER registers is taken from the input register and buffered by inverting and non-inverting IC's. The output of these buffers are routed to the DER inputs and determine whether the DER's output will be positive or negative true data. Calibration data is sent to a third buffer that is controlled by the CALIBRATION mode of the DAC021.

1.3.2 CPI012

Figure 1-2 is a block diagram of the CPI012 module. The CPI012 module accepts parallel data, sync status, minor and major strobes from the frame sync module. The parallel data is buffered by FIFO's and output to either one of two DRB32W interfaces.

The parallel data from the frame sync is stored in a register by the word strobe of the frame sync. The output of this register is applied to the FIFO. The FIFO input control logic determines when and if the parallel data is to be loaded. Writing data into the FIFO will occur when the selected status state of the frame synchronizer has been achieved and the appropriate boundary pulse has been received. The status state (transfer criteria) and boundary pulse (buffer begins - minor or major frame) are selected by the user based on his system requirements.

The output of data from the FIFO is controlled by the DRB32W interface through the FIFO output control logic. The fact that the FIFO is not empty and the DRB32W interface is ready to accept data causes the control logic to read data from the FIFO. The output from the FIFO is stored in a register. Its output is applied to each of the two output interface buffers only one of which will be enabled (user selection).

If channel 1 is selected as the PRIME channel, then the input and output data and control signals from DRB32W interface number one will be active. If channel 2 is selected, its input and output signals will be active.

If the FIFO input control logic detects that the FIFO becomes full, it will halt any further writing of data to the FIFO. This is a latched condition which requires a reset to be generated before it can be cleared. If the FIFO output control logic detects an empty FIFO, it will suspend any further transfers to the DRB32W until a word(s) is written into the FIFO. As soon as the empty flag is cleared by the FIFO, the output control logic will resume data transfers to the DRB32W.

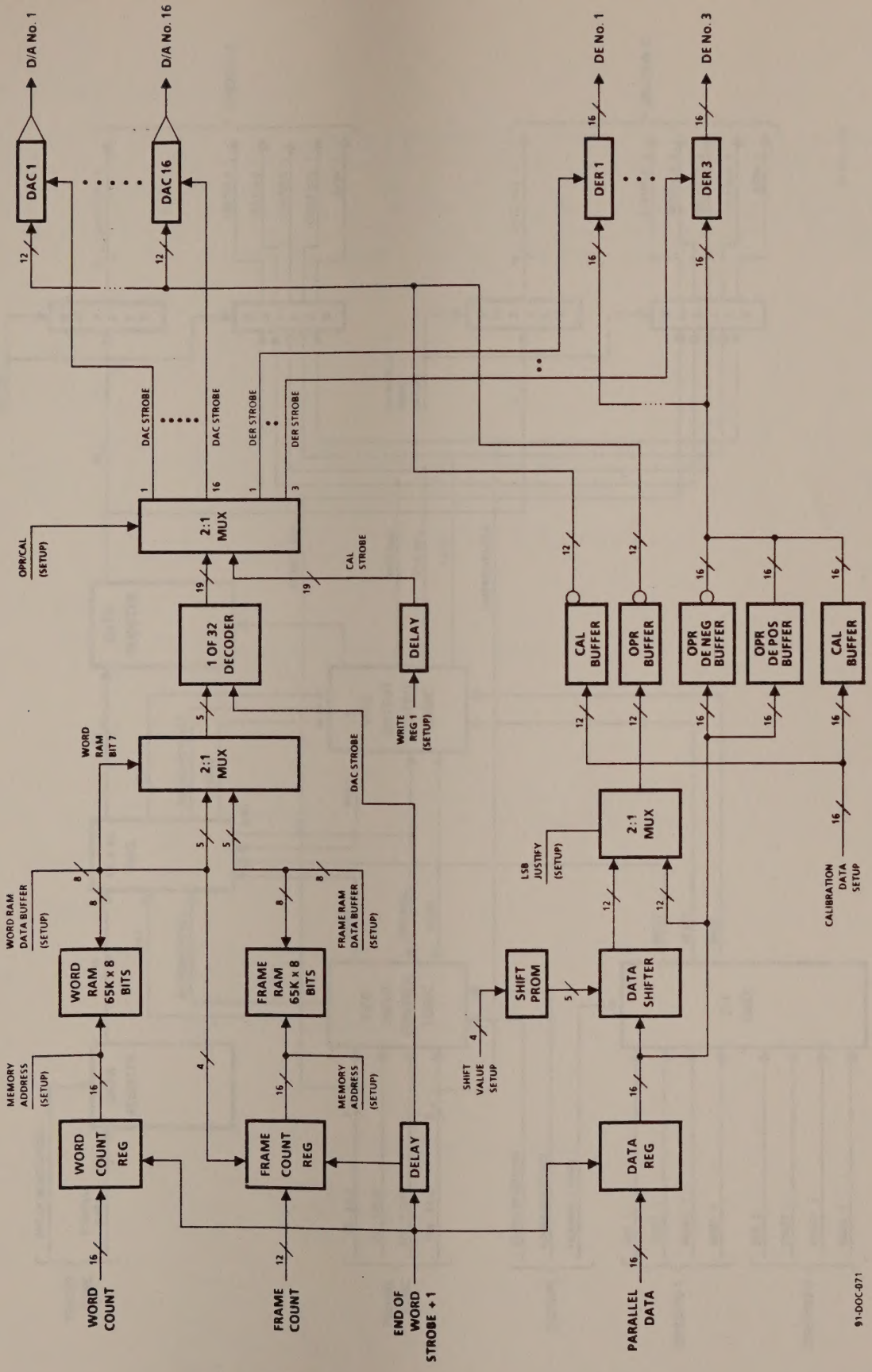
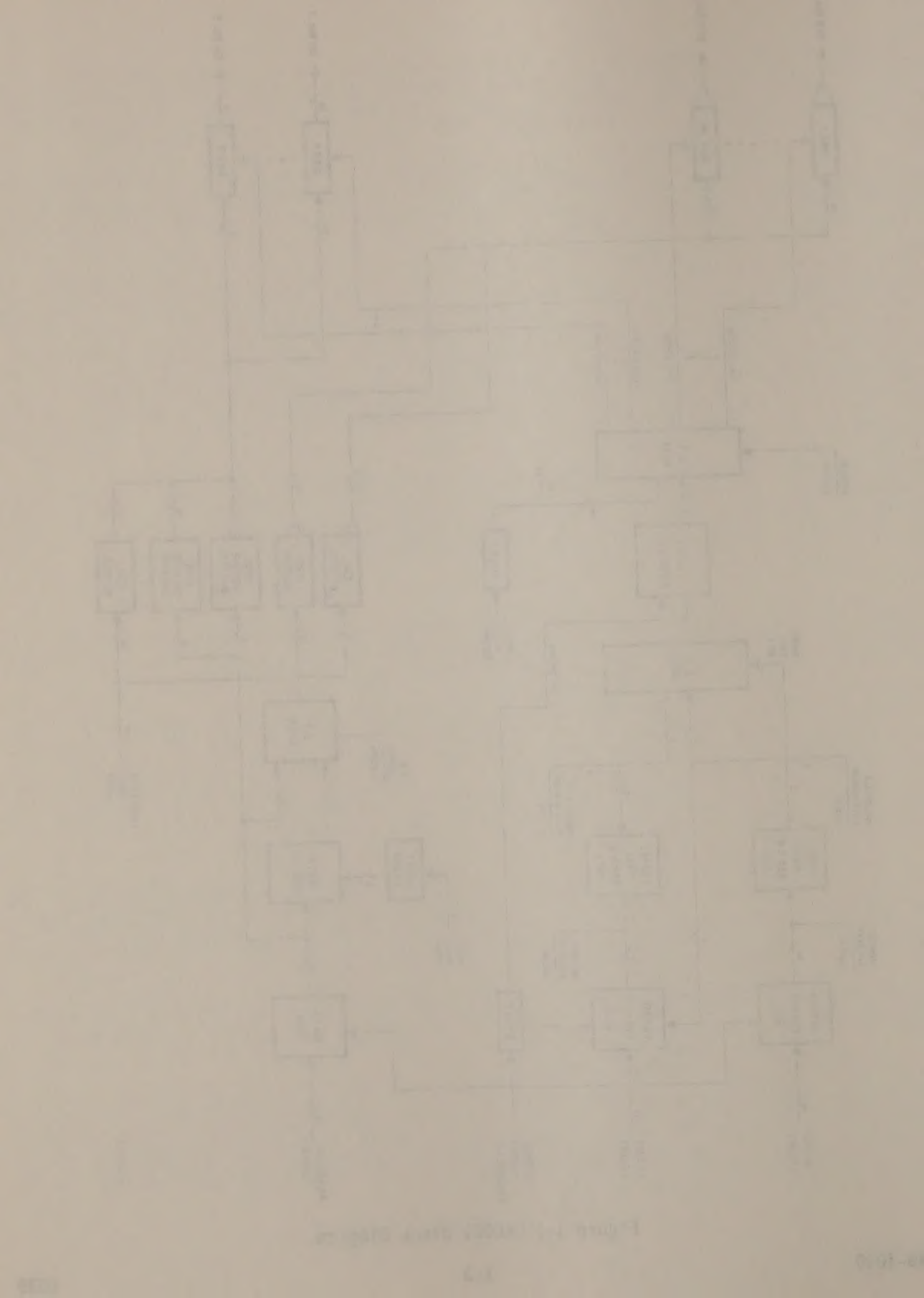


Figure 1-1 DAC021 Block Diagram



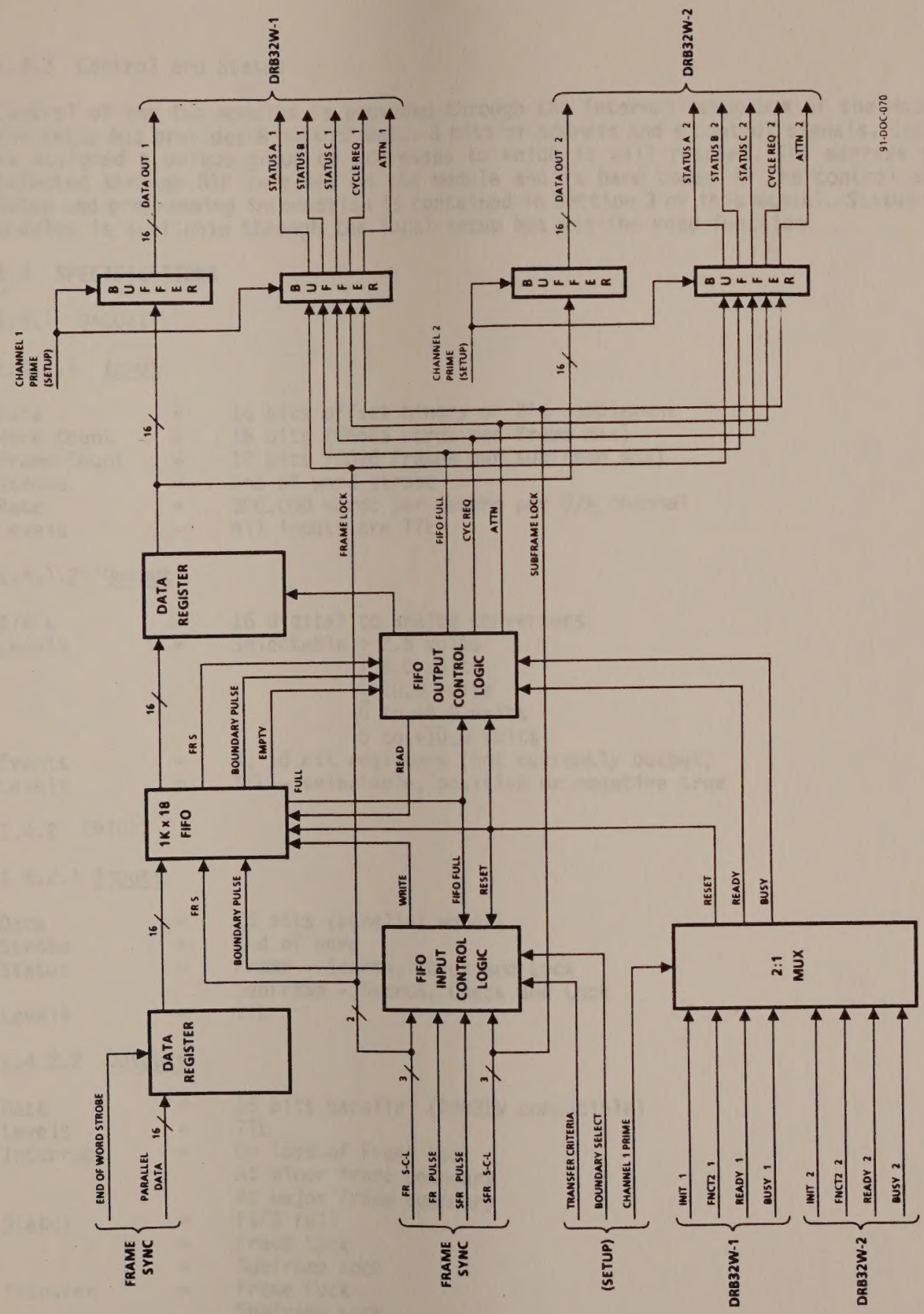
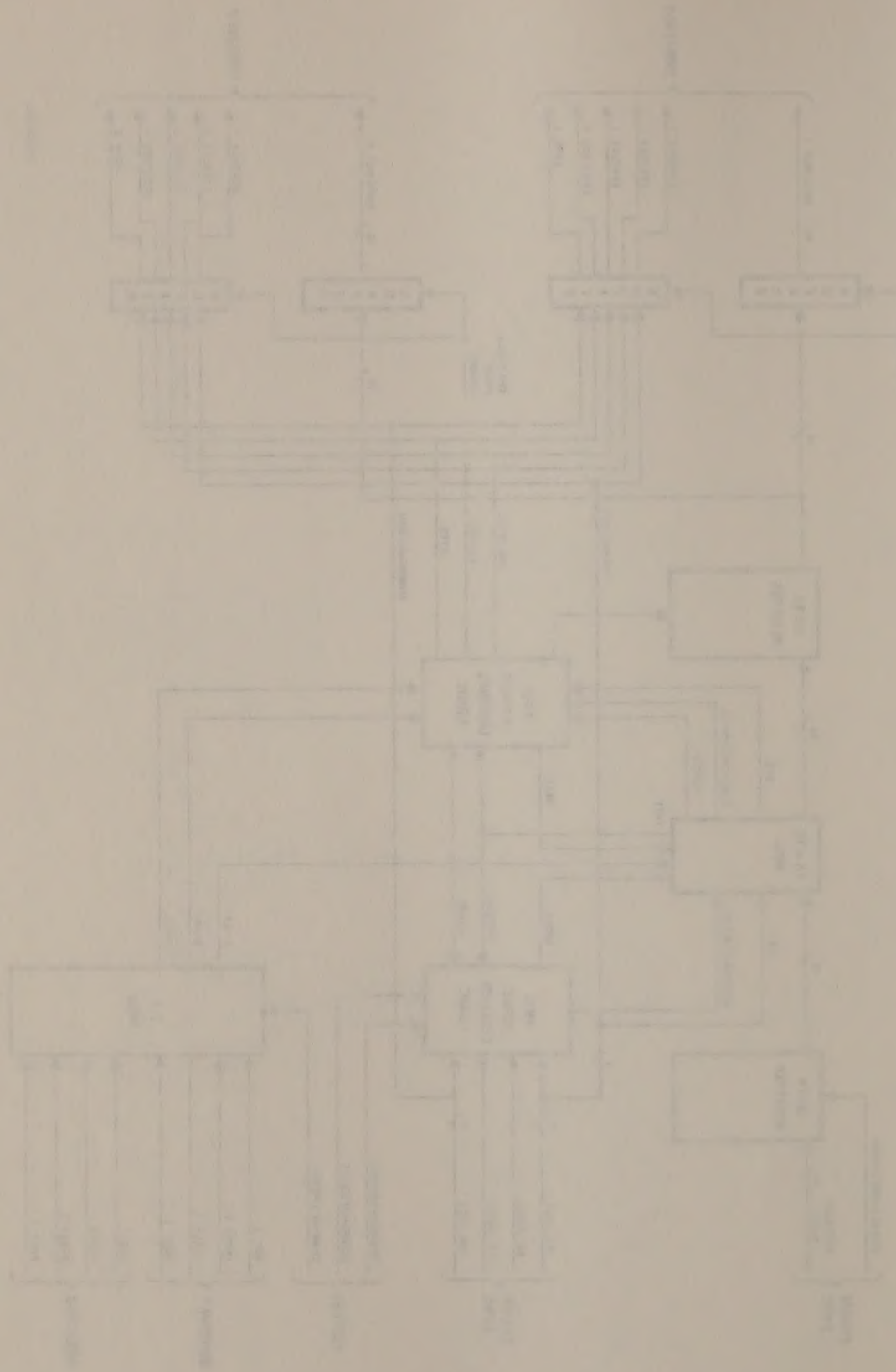


Figure 1-2 CPI012 Block Diagram



1.3.3 Control and Status

Control of the two modules is provided through the internal setup bus of the Model 3440. The setup bus provides 8 bits of data, 8 bits of address and 4 control signals. Each module is assigned a unique group of addresses to which it will respond. The address group is selected through DIP switches on the module and is hard coded in the control software. Setup and programming information is contained in Section 3 of this manual. Status of these modules is available through the local setup bus via the read function.

1.4 SPECIFICATIONS

1.4.1 DAC021

1.4.1.1 Input

Data	=	16 bits offset binary or 2's complement
Word Count	=	16 bits (65535 words per frame max)
Frame Count	=	12 bits (4096 frames per subframe max)
Strobe	=	End of word strobe
Rate	=	300,000 words per second per D/A channel
Levels	=	All inputs are TTL

1.4.1.2 Output

D/A's	=	16 digital to analog converters
Levels	=	Selectable ± 2.5 volts
		± 5.0 volts
		± 10.0 volts
		0 to +5.0 volts
		0 to +10.0 volts
Events	=	3, 16 bit registers (not currently output)
Levels	=	TTL - selectable, positive or negative true

1.4.2 CPI012

1.4.2.1 Inputs

Data	=	16 bits (parallel words)
Strobe	=	End of word
Status	=	Frame - Search, Check and Lock
		Subframe - Search, Check and Lock
Levels	=	TTL

1.4.2.2 Outputs

Data	=	16 bits parallel (DRB32W compatible)
Levels	=	TTL
Interrupt	=	On loss of Frame Lock
		At minor frame boundary
		At major frame boundary
Status	=	FIFO full
	=	Frame Lock
	=	Subframe Lock
Transfer	=	Frame Lock
		Subframe Lock
		Both Lock
		Frame not in Search

Subframe not in Search
Both not in Search
Always - ignore synchronizer's status states

Rate = Maximum transfer rate of DRB32W interface

Section 2
INSTALLATION

2.0 GENERAL

The two modules are supplied as part of the Model 3440 and are located in slots 5 and 7 (DAC021 and CPI012 respectively). The output connector pin assignments are contained in the next paragraph. Setup and programming information is contained in section 3 of this addendum.

2.1 CONNECTOR PIN ASSIGNMENTS

The pin assignments for each of the rear panel connectors associated with the DAC021 and the CPI012 are shown under this paragraph.

2.1.1 DAC021

The outputs from the DAC021 are contained in a single 50 pin connector located on the rear of the Model 3440. It is identified as J15. Its pin assignments are given in Table 2-1.

Table 2-1 DAC021 Digital to Analog Converter Module Outputs

Reference Designation: J15

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
01	GND	D/A 1 RETURN	18	DAC9	D/A 9 SIGNAL
02	DAC1	D/A 1 SIGNAL	19	GND	D/A 10 RETURN
03	GND	D/A 2 RETURN	20	DAC10	D/A 10 SIGNAL
04	DAC2	D/A 2 SIGNAL	21	GND	D/A 11 RETURN
05	GND	D/A 3 RETURN	22	DAC11	D/A 11 SIGNAL
06	DAC3	D/A 3 SIGNAL	23	GND	D/A 12 RETURN
07	GND	D/A 4 RETURN	24	DAC12	D/A 12 SIGNAL
08	DAC4	D/A 4 SIGNAL	25	GND	D/A 13 RETURN
09	GND	D/A 5 RETURN	26	DAC13	D/A 13 SIGNAL
10	DAC5	D/A 5 SIGNAL	27	GND	D/A 14 RETURN
11	GND	D/A 6 RETURN	28	DAC14	D/A 14 SIGNAL
12	DAC6	D/A 6 SIGNAL	29	GND	D/A 15 RETURN
13	GND	D/A 7 RETURN	30	DAC15	D/A 15 SIGNAL
14	DAC7	D/A 7 SIGNAL	31	GND	D/A 16 RETURN
15	GND	D/A 8 RETURN	32	DAC16	D/A 16 SIGNAL
16	DAC8	D/A 8 SIGNAL	33-50	-----	NOT USED
17	GND	D/A 9 RETURN			

2.1.2 CPI012

The outputs from the CPI012 consist of two identical groups of signals. Each group is intended to be connected to a DRB32W interface in a DEC computer. The Channel 1 output is assigned to connectors J11 and J12 and the Channel 2 output is assigned to connectors J13 and J14.

Table 2-2 Channel 1 DRB32W Output Interface

Reference Designation: J11

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
01	GND		14	1-STATUS B(+) Status B	
02	1-CYC REQ(+)	Cycle Request	15	GND	
03	GND		16	1-STATUS C(+)	Status C
04	1-FNCT 2(+)	Function 2	17	GND	
05	GND		18	1-STATUS C(+)	Status C
06	1-READY(-)	Ready	19	GND	
07	GND		20	----	
08	1-WC INC ENB(+)	Word Count Increment Enable	21	GND	
09	1-BURST RQ(+)	Burst Request	22	----	
10	1-STATUS A(+)	Status A	23	GND	
11	GND		24	GND	
12	1-INIT(+)	Initialize	25-40	----	
13	GND				

Table 2-3 Channel 1 DRB32W Output Interface

Reference Designation: J12

PIN	NAME	PIN	NAME
01	GND	21	GND
02	1-BUSY(+)	22	GND
03	GND	23	GND
04	1-ATTN(+)	24	GND
05	GND	25	1-DATA 7(+)
06	1-AOO(+)	26	1-DATA 8(+)
07	GND	27	1-DATA 6(+)
08	1-BA INC ENB(+)	28	1-DATA 9(+)
09	----	29	1-DATA 5(+)
10	----	30	1-DATA 10(+)
11	GND	31	1-DATA 4(+)
12	1-CO(+)	32	1-DATA 11(+)
13	GND	33	1-DATA 3(+)
14	1-FNCT 2(+)	34	1-DATA 12(+)
15	GND	35	1-DATA 2(+)
16	1-C1(+)	36	1-DATA 13(+)
17	GND	37	1-DATA 1(+)
18	----	38	1-DATA 14(+)
19	GND	39	1-DATA 0(+)
20	---	40	1-DATA 15(+)

Table 2-4 Channel 2 DRB32W Output Interface

Reference Designation: J13

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
01	GND		14	2-STATUS B(+)	Status B
02	2-CYC REQ(+)	Cycle Request	15	GND	
03	GND		16	2-STATUS C(+)	Status C
04	2-FNCT 2(+)	Function 2	17	GND	
05	GND		18	2-STATUS C(+)	Status C
06	2-READY(-)	Ready	19	GND	
07	GND		20	----	
08	2-WC INC ENB(+)	Word Count Increment Enable	21	GND	
09	2-BURST RQ(+)	Burst Request	22	----	
10	2-STATUS A(+)	Status A	23	GND	
11	GND		24	GND	
12	2-INIT(+)	Initialize	25-40	----	
13	GND				

Table 2-5 Channel 2 DRB32W Output Interface

Reference Designation: J14

PIN	NAME	PIN	NAME
01	GND	21	GND
02	2-BUSY(+)	22	GND
03	GND	23	GND
04	2-ATTN(+)	24	GND
05	GND	25	2-DATA 7(+)
06	2-A00(+)	26	2-DATA 8(+)
07	GND	27	2-DATA 6(+)
08	2-BA INC ENB(+)	28	2-DATA 9(+)
09	----	29	2-DATA 5(+)
10	----	30	2-DATA 10(+)
11	GND	31	2-DATA 4(+)
12	2-C0(+)	32	2-DATA 11(+)
13	GND	33	2-DATA 3(+)
14	2-FNCT 2(+)	34	2-DATA 12(+)
15	GND	35	2-DATA 2(+)
16	2-C1(+)	36	2-DATA 13(+)
17	GND	37	2-DATA 1(+)
18	----	38	2-DATA 14(+)
19	GND	39	2-DATA 0(+)
20	---	40	2-DATA 15(+)

Table 2-6 Status Outputs

PIN	NAME	DESCRIPTION
J5-1	FRM CLK(+)	End of Frame Pulse (+) differential
J5-2	FRM CLK(-)	End of Frame Pulse (-) differential
J5-3	SHIELD	Chassis Ground
J6-1	SFRM CLK(+)	End of Subframe Pulse (+) differential
J6-2	SFRM CLK(-)	End of Subframe Pulse (-) differential
J6-3	SHIELD	Chassis Ground
J7-1	FR LOCK(+)	Frame Lock Status (+) differential
J7-2	FR LOCK(-)	Frame Lock Status (-) differential
J7-3	SHIELD	Chassis Ground

The differential signals FRM CLK and SFRM CLK are negative going active signals so that they normally sit in a high state and go low when active.

Section 3
OPERATION

3.0 INTRODUCTION

This section contains the operating information for the DAC021 and the CPI012 modules. The information consists of the local display pages, internal registers, the IEEE-488 PID-PAR definitions and selection of the D/A output voltage level.

3.1 CONTROLS AND INDICATORS

The 3440 front panel controls and indicators explained in Table 3-1.

Table 3-1. 3440 Front Panel LEDs

NAME	TYPE	FUNCTION
DATA	GRN	Data transitions detected
CLOCK	GRN	Clock transitions detected
SLIP	RED	Frame slip detected
PARITY ERROR	RED	Parity error in a word detected
INVERTED DATA	YEL	APC is active and Complemented data detected
FR BYPASS	YEL	Always generate parallel data
PRIME/ STANDBY	GRN	On when prime interface is active, Off when standby interface is active
FR SEARCH	RED	Frame sync in Search state
FR CHECK	YEL	Frame sync in Check state
FR LOCK	GRN	Frame sync in Lock state
FR FLYWHEEL	YEL	Frame sync still in Lock but Flywheeling
SFR SEARCH	RED	Subframe sync in Search state
SFR CHECK	YEL	Subframe sync in Check state
SFR LOCK	GRN	Subframe sync in Lock state
SFR FLYWHEEL	YEL	Subframe sync still in Lock but Flywheeling

3.2 NORMAL OPERATING PROCEDURES

Normal operating instructions include the powering up or down procedures and local or remote operating modes.

3.2.1 POWER UP OR DOWN PROCEDURES

There are no special procedures for applying power to or removing power from the 3440. Power is applied by placing the AC rocker switch in the up position and power is removed by placing the switch in the down position. When power is first applied, a power on sequence is executed. This sequence includes: a) memory test, b) load the current format, c) display the STATUS page. When power is removed, the current format is saved.

3.2.2 RESETTING THE 3440

To initiate a power on reset sequence, press the RESET key and then press the ENTER key.

3.2.3 SELECTING A DISPLAY PAGE

A page is selected by pressing the PAGE key followed by pressing the Right arrow (increment) or Left arrow (Decrement), or by pressing the appropriate numeric key (0 through 9). For Pages above Page 9 press the PAGE key, followed by the FCTN key, followed by the corresponding alphanumeric key (A through F).

3.2.4 LOCAL AND REMOTE MODES

In local, the format parameters of the 3440 are updated via the various setup display pages. The current setup and status information are displayed on these pages and are available to the remote control interface. Setup commands from the remote interface are ignored.

When the remote mode is selected, the format parameters are setup through the active remote interface. All setup and status information is available to the remote user. Only the status page and the switches setup page are available to the front panel display.

3.2.4.1 Selecting Local or Remote. Local or remote is selected by the LCL/RMT field on the Switches Page (Page 1). When this field is set to LOCAL, the 3440 is in local control. Remote control is enabled when this field is set to REMOTE. See 3.3.2 for a description of how to change the parameter in this type of field.

3.2.4.2 Common Local/Remote Parameter List. A single parameter list is used to control the 3440. The LCL/RMT field merely selects the source of updates to this list. So, the action of switching from local to remote or vice-versa will not disturb the current format. If the 3440 is remotely setup and then returned to local control, the display setup pages will reflect the current parameter list.

3.3 LOCAL OPERATION

3.3.1 MENU OF DISPLAY PAGES

PAGE 0	STATUS
PAGE 1	SWITCHES
PAGE 2	GENERAL SETUP
PAGE 3	FS PATTERN SETUP
PAGE 4	FRAME SYNC SETUP
PAGE 5	ID COUNTER SETUP
PAGE 6	SUBFRAME SYNC SETUP
PAGE 7	FSP ERR ACCUM/DC SETUP
PAGE 8	TEST PATTERN SETUP
PAGE 9	DAC/CAL CONTROL
PAGE 10	DAC SETUP
PAGE 11	DER SETUP
PAGE 12	DR32W INTERFACE SETUP

3.3.2 KEY FIELD

Each display page uses the last character location on the first line to distinguish between STEP parameters and NUMERIC parameters. Also, this field is used to indicate when a special key (PAGE, RESET or FCTN) has been pressed.

3.3.3 CHANGING A STEP FIELD ON ANY PAGE

A step field is one that has a defined set of parameters.

a. Use an ARROW key to select the field. A field is selected when the current parameter setting flashes.

b. Step through the set of parameters by pressing the FCTN key.

c. If the LEFT ARROW key is pressed, the old parameter is automatically retained and the previous field is selected.

d. If the RIGHT ARROW key is pressed, the old parameter is automatically retained and the next field is selected.

e. When the desired parameter appears on the display, press the ENTER key to load it.

3.3.4 CHANGING A NUMERIC FIELD ON ANY PAGE

A numeric field is one that has a defined range of numbers.

a. Use an ARROW key to select the field. A field is selected when the current number setting flashes.

b. Enter a number by pressing the appropriate numeric keys. To enter HEX values A through F that appear above the numeric keys, press the FCTN key and then the numeric key.

c. The LEFT ARROW key is used to delete modified characters toward the left most character in the number. If the LEFT ARROW key is pressed beyond the left most character, the old number is automatically retained and the previous field is selected.

d. If the RIGHT ARROW key is pressed, the old number is automatically retained and the next field is selected.

e. When the desired number appears on the display, press the ENTER key to load it.

3.3.5 CHANGING A SPECIAL FIELD ON PAGE 3

The PATTERN field and the MASK field are special fields. Each field is divided into 16 sub-fields. The sub-fields hold HEX values between 0 and F.

a. Use an ARROW key to select a sub-field. A sub-field is selected when the current HEX value flashes.

b. Enter a HEX value by pressing the appropriate numeric keys. To enter HEX values A through F that appear above the numeric keys, press the FCTN key and then the numeric key. Entering a value causes the next sub-field to be selected.

c. If the LEFT ARROW key is pressed when sub-field 1 is selected, the old HEX values are automatically retained and the previous field is selected.

d. If the RIGHT ARROW key is pressed when sub-field 16 is selected, the old HEX values are automatically retained and the next field is selected.

e. When the desired HEX values appear in the field, press the ENTER key to load the new pattern into the correlator.

3.3.6 LOADING DAC OR DER INFORMATION

To enter individual DAC or DER information you must:

a. Select the number of the DAC or DER [DAC # :].

b. Select the number of the WORD that is to be routed to the DAC [WORD # :].

c. Select the number of the FRAME in which the word is located if the word is sub-commutated [FRAME # :].

d. Select the WORD INTERVAL [WORD INTERVAL :] when the word is supercommutated.

e. Select the FRAME INTERVAL [FRAME INTERVAL :] when the word is sub-supercommutated.

f. When in the [LOAD : (ENTER)] field, press the ENTER key to store the information for the selected DAC.

NOTE: This does not load the DAC circuitry. This loads the information into RAM on the IOC module where it is now available to be loaded into the DAC.

To load DAC or DER information you must:

a. With the cursor in the [DAC # :] field, press the FNCT key then press the ENTER key.

3.3.7 DESCRIPTION OF DISPLAY PAGES

3.3.7.1 Fields on the STATUS Page

```
*****************************************
*            PAGE 0  STATUS             *
*LCL/RMT    =          SOURCE SEL =      *
*FRAME SLIP =          APC =             *
*PARITY     =                            *
*FSP ERRS   =                            *
*DC WORD    =                            *
*****************************************
```

FIELD NAME	TYPE	ALLOWABLE VALUES	DESCRIPTION
LCL/RMT	STATUS	LOCAL	Unit is in LOCAL CONTROL MODE
		REMOTE	Unit is in REMOTE CONTROL MODE
SOURCE SEL	STATUS	A	Unit is processing SOURCE A
		TEST	Internal simulated data is selected
FRAME SLIP	STATUS	+1/-1/+2/-2/+3/-3	Detected BIT SLIP MAGNITUDE and DIRECTION Bits
		(BLANK)	NO BIT SLIP
APC	STATUS	POSITIVE	Detected data is NORMAL POLARITY
		NEGATIVE	Detected data is INVERTED POLARITY (APC MODE Only)
PARITY	STATUS	ERROR	PARITY ERROR Detected
		(BLANK)	NO PARITY ERROR Detected
FSP ERRS	STATUS	0 to 150,000 Bits	Accumulated MINOR FRAME SYNC PATTERN ERRORS
DC WORD	STATUS	0 to 111111111111-1111 (BIN)	DISPLAY of SELECTED DATA CAPTURE WORD
		0 to 177777 (OCT)	
		0 to 65535 (DEC)	
		0 to FFFF (HEX)	

3.3.7.2 Fields on the SWITCHES Page

```
*****************************************
*           PAGE 1  SWITCHES            *
*LCL/RMT       =                        *
*FRMT NUMBER   =     FRMT FUNCTION =    *
*488 ADDRESS   =                        *
*PSI LO CODE   =       PSI HI CODE =    *
*                                       *
*****************************************
```

FIELD NAME	TYPE	ALLOWABLE VALUES	DESCRIPTION
LCL/RMT	STEP	LOCAL	Enables Front Panel control of the unit
		REMOTE	Enables REMOTE CONTROL of the unit
FRMT NUMBER	NUMERIC	1 to 8	Select FORMAT Number to be used on SAVE or LOAD
FRMT FUNCTION	STEP	NONE	No Format action
		LOAD	Load stored Format into current setup
		SAVE	Save current setup into Stored Format
488 ADDRESS	NUMERIC	0 to 31	IEEE-488 Remote Control Port Listen Address
PSI LO CODE	NUMERIC	0 to F	Parallel Remote Control Port Addresses (2 unit addresses are assigned to the 3440)
PSI HI CODE	NUMERIC	0 to F	

3.3.7.3 Fields on the GENERAL SETUP Page

```
*****************************************
*         PAGE 2  GENERAL SETUP         *
*INPUT SEL    =                        *
*DATA POL SEL =                 APC =   *
*FRAME LENGTH =                        *
*WORD LENGTH  =          ORIENTATION =  *
*PARITY MODE  =        PARITY STRIP =   *
*****************************************
```

FIELD NAME	TYPE	ALLOWABLE VALUES	DESCRIPTION
INPUT SEL	STEP	A	Select INPUT PORT A
		TEST	Select INTERNAL SIMULATOR
DATA POL SEL	STEP	NORM	Do NOT Invert INPUT DATA
		INV	Invert INPUT DATA
APC	STEP	ON	AUTOMATIC POLARITY CORRECTION Enabled
		OFF	AUTOMATIC POLARITY CORRECTION Disabled
FRAME LENGTH	NUMERIC	8 to 65536	MINOR FRAME LENGTH in BITS
WORD LENGTH	NUMERIC	1 to 16	DATA WORD LENGTH in BITS
ORIENTATION	STEP	LSB	LSB of DATA WORD Received First
		MSB	MSB of DATA WORD Received First
PARITY MODE	STEP	NONE	NO PARITY CHECK
		EVEN	CHECK EVEN PARITY
		ODD	CHECK ODD PARITY
PARITY STRIP	STEP	NONE	NO PARITY STRIP
		MSB	STRIP MSB
		LSB	STRIP LSB

3.3.7.4 Fields on the FS PATTERN SETUP Page

```
*****************************************
*       PAGE 3  FS PATTERN SETUP        *
*LOCATION =                             *
*TYPE     =                             *
*PATTERN  =                             *
*MASK     =                             *
*                                       *
*****************************************
```

FIELD NAME	TYPE	ALLOWABLE VALUES	DESCRIPTION
LOCATION	STEP	FIRST	Minor Frame Sync Pattern is First Word in Frame
		LAST	Minor Frame Sync Pattern is Last Word in Frame
TYPE	STEP	NORMAL	All occurrences of Minor Frame Sync Pattern are Normal Polarity
		AFS	Minor Frame Sync Pattern Alternates Polarity Every Frame
		CFS	Minor Frame Sync Pattern Complements at the Major Frame Rate
PATTERN	SPECIAL	16 HEX CHARACTERS	Minor Frame Sync Pattern
MASK	SPECIAL	16 HEX CHARACTERS	Minor Frame Sync Pattern Mask
			MASK BIT = 1 PATTERN BIT USED
			MASK BIT = 0 PATTERN BIT UNUSED

3.3.7.4.1 Setting up the PATTERN Field and the MASK Field. The Frame Sync Pattern orientation in the PATTERN Field determines how the pattern will appear in the correlators. When the pattern is FIRST (selected by the LOCATION field) the first bit of the pattern that is received must be the MSB of the HEX value in sub-field 1. When the pattern is LAST, the last bit of the pattern that is received must be the LSB of the HEX value in sub-field 16.

Once the PATTERN field is specified, the MASK field can be entered. Each bit position in the PATTERN field that is to be compared to the input serial data must have that bit position in the MASK field set to a one.

Example:
Specify the Frame Sync Pattern.

The pattern is specified from left to right. The left most bit is the first bit of the pattern that will be received and the right most bit is the last bit of the pattern that will be received.

10010110101001011111000000111 1

LOCATION = FIRST

The HEX representation of the pattern is found by segmenting the bits into groups of four starting with the left most bit. The left most bit of a segment is the most significant bit. If there are less than four bits in the last segment, place zeroes in the least significant bit positions of the segment.

```
1001 0110 1010 0101 1111 0000 0011 11
1001 0110 1010 0101 1111 0000 0011 1100
 9    6    A    5    F    0    3    C
```

The HEX values are entered into the PATTERN field as follows:

PATTERN SUB-FIELDS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
9	6	A	5	F	0	3	C	0	0	0	0	0	0	0	0

If all of the bits in the pattern are to be compared with the serial data, the MASK field is entered as follows:

MASK SUB-FIELDS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
F	F	F	F	F	F	F	C	0	0	0	0	0	0	0	0

LOCATION = LAST

The HEX representation of the pattern is found by segmenting the bits into groups of four starting with the right most bit. The left most bit of a segment is the most significant bit. If there are less than four bits in the last segment, place zeroes in the most significant bit positions of the segment.

```
  10 0101 1010 1001 0111 1100 0000 1111
0010 0101 1010 1001 0111 1100 0000 1111
 2    5    A    9    7    C    0    F
```

The HEX values are entered into the PATTERN field as follows:

PATTERN SUB-FIELDS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	0	0	0	0	0	2	5	A	9	7	C	0	F

If all of the bits in the pattern are to be compared with the serial data, the MASK field is entered as follows:

MASK SUB-FIELDS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	0	0	0	0	0	3	F	F	F	F	F	F	F

3.3.7.5 Fields on the FRAME SYNC SETUP Page

```
*****************************************
*       PAGE 4  FRAME SYNC SETUP        *
*FR SYNC   =                            *
*MODE      =                            *
*MED       =             WINDOW     =   *
*SRCH ERRS =             CHECK PTNS =   *
*LOCK ERRS =             LOCK PTNS  =   *
*****************************************
```

FIELD NAME	TYPE	ALLOWABLE VALUES	DESCRIPTION
FR SYNC	STEP	ON	Minor Frame Sync Enabled
		OFF	Minor Frame Sync Disabled
		BYPASS	Minor Frame Sync Disabled but Serial-to-Parallel Converter and Output Interface Enabled
MODE	STEP	NORMAL	Use Normal Sync Strategy (SRCH ERRS & CHECK PTNS) to Advance to LOCK
		QUICK	Advance from SEARCH to LOCK Immediately if detected Minor Frame Sync Pattern has Zero Errors Regardless of Sync Strategy(SRCH ERRS & CHECK PTNS)
MED	STEP	ON	Minimum Error Detection Enabled. Finds Minor Frame Sync Pattern with Minimum number of errors during First Check Frame

FIELD NAME	TYPE	ALLOWABLE VALUES	DESCRIPTION
		OFF	Minimum Error Detection Disabled. Syncs to First Acceptable Minor Frame Sync Pattern
WINDOW	STEP	0	No Bit Slip Allowed
		± 1	Allows Slip of +/-1 Bit
		± 2	Allows Slip of +/-2 Bits
		± 3	Allows Slip of +/-3 Bits
SRCH ERRS	NUMERIC	0 to 15	Minor Frame Sync Pattern Bit Error Tolerance in SEARCH and CHECK Modes
LOCK ERRS	NUMERIC	0 to 15	Minor Frame Sync Pattern Bit Error Tolerance in LOCK and FLYWHEEL Modes
CHECK PTTNS	NUMERIC	0 to 15	Number of Check Frames between SEARCH and LOCK. This number of consecutive acceptable (within Error tolerance) Minor Frame Sync Patterns MUST be found BEFORE Advancing to LOCK
LOCK PTTNS	NUMERIC	0 to 15	Number of FLYWHEEL Frames between LOCK and SEARCH. This number of consecutive unacceptable (exceeding Error tolerance) Minor Frame Sync Patterns MUST be found BEFORE Returning to SEARCH

3.3.7.6 Fields on the ID COUNTER SETUP Page

```
*****************************************
*       PAGE 5  ID COUNTER SETUP        *
*COUNT DIR   =                          *
*MIN COUNT   =         MAX COUNT   =    *
*ID WORD LEN =         ORIENTATION =    *
*  * LOCATION OF LAST ID BIT RECEIVED *  *
*WORD NUMBER =         BIT NUMBER  =    *
*****************************************
```

FIELD NAME	TYPE	ALLOWABLE VALUES	DESCRIPTION
COUNT DIR	STEP	UP	ID Counter Increments
		DOWN	ID Counter Decrements
MIN COUNT	STEP	0	Minimum ID Count is 0
		1	Minimum ID Count is 1
MAX COUNT	NUMERIC	2 to 4095	Maximum ID Count Value
ID WORD LEN	NUMERIC	1 to 12	ID Counter Word Length in Bits
ORIENTATION	STEP	LSB	LSB of ID Counter Word Received First
		MSB	MSB of ID Counter Word Received First
WORD NUMBER	NUMERIC	0 to (Frame Length/Word Length)-1	The Word which contains the Last Bit Received of the ID Counter Word
BIT NUMBER	NUMERIC	0 to (Word Length -1)	The Bit in the above Word which contains the Last Bit Received of the ID Counter Word (Bit Number = 0 corresponds to first bit of word received, regardless of word orientation)

3.3.7.7 Fields on the SUBFRAME SYNC SETUP Page

```
*****************************************
*      PAGE 6  SUBFRAME SYNC SETUP      *
*SF SYNC    =                           *
*MODE       =                           *
*CHECK ERRS =            CHECK PTNS =   *
*LOCK ERRS  =            LOCK PTNS  =   *
*                                       *
*****************************************
```

FIELD NAME	TYPE	ALLOWABLE VALUES	DESCRIPTION
SF SYNC	STEP	ON	Subframe Sync Enabled
		OFF	Subframe Sync Disabled
MODE	STEP	ID	Synchronize to Incrementing or Decrementing ID Counter
		JAM	Jam Synchronizer with ID Word (Need not be Incrementing or Decrementing)
		CFS	Synchronize to Complementing Minor Frame Sync Pattern
CHECK ERR	NUMERIC	0 to 7	ID Counter Bit Error Tolerance in CHECK Mode
LOCK ERR	NUMERIC	0 to 7	ID Counter Bit Error Tolerance in LOCK and FLYWHEEL Mode
CHECK PTNS	NUMERIC	0 to 15	Number of Check Frames between SEARCH and LOCK. This number of consecutive acceptable ID counts must be found before advancing to LOCK.
LOCK PTNS	NUMERIC	0 to 15	Number of FLYWHEEL Frames between LOCK and SEARCH. This number of consecutive unacceptable ID counts must be found before returning to SEARCH.

3.3.7.8 Fields on the FSP ERR ACCUM / DC SETUP Page

```
*****************************************
*   PAGE 7  FSP ERR ACCUM / DC SETUP    *
*FSP ERR LEN =                          *
*DC FORMAT   =                          *
*DC MODE     =                          *
*WORD #      =            FRAME # =     *
*DC WORD     =                          *
*****************************************
```

FIELD NAME	TYPE	ALLOWABLE VALUES	DESCRIPTION
FSP ERR LEN	STEP	1/10/100/1000/ 10000	Number of Frames over which Minor Frame Sync Pattern Errors are accumulated for display
DC FORMAT	STEP	BIN OCT DEC HEX	Data Capture Word displayed in Binary, Octal, Decimal or Hexadecimal
DC MODE	STEP	MINOR FRAME	Captures Specified Word out of the Minor Frame without regard for Frame Number
		MAJOR FRAME	Captures Specified Word out of the Major Frame using both Word # and Frame #
WORD #	NUMERIC	0 to (FRAME LENGTH/WORD LENGTH)-1	Word Number of Data to be captured
FRAME #	NUMERIC	ID MIN COUNT to ID MAX COUNT	Frame Number of Data to be captured
DC WORD	STATUS	0 to 111111111111-1111 (BIN) 0 to 177777 (OCT) 0 to 65535 (DEC) 0 to FFFF (HEX)	Local display of Data Capture Word Updates only when cursor is in field

3.3.7.9 Fields on the TEST PATTERN SETUP Page

```
*****************************************
*      PAGE 8  TEST PATTERN SETUP       *
*PTTN SELECT =                          *
*RATE        =                          *
*WORD LEN    =          WORDS/FRM =     *
*                                       *
*                                       *
*****************************************
```

FIELD NAME	TYPE	ALLOWABLE VALUES	DESCRIPTION
PTTN SELECT	STEP	0/1/2/3	Select Test Pattern
RATE	STEP	OSC/2, OCS/4, OSC/8, OSC/16, OSC/32, OSC/64, OSC/128, OSC/256	Select Test Pattern Data Rate OSC = 40 MHz
WORD LEN	NUMERIC	8 to 16	Select Test Pattern Word Length in Bits
WORDS/FRM	NUMERIC	1 to 4096	Select Test Pattern Frame Length in Words

3.3.7.10 Default Formats

The 3440 is shipped from the factory so that the following format is automatically loaded when the unit is powered-up.

```
*****************************************
*           PAGE 1  SWITCHES            *
*LCL/RMT       = LOCAL                  *
*FRMT NUMBER   = 1   FRMT FUNCTION = NONE*
*488 ADDRESS   = 0                      *
*PSI LO CODE   = 0     PSI HI CODE = 1  *
*                                       *
*****************************************
```

```
*******************************************
*         PAGE 2  GENERAL SETUP           *
*INPUT SEL    = TEST                      *
*DATA POL SEL = NORM            APC = OFF*
*FRAME LENGTH = 512                       *
*WORD LENGTH  = 16      ORIENTATION = MSB*
*PARITY MODE  = NONE  PARITY STRIP = NONE*
*******************************************

*******************************************
*       PAGE 3  FS PATTERN SETUP          *
*LOCATION = LAST                          *
*TYPE     = CFS                           *
*PATTERN  = 000000000000FAF3              *
*MASK     = 000000000000FFFF              *
*                                         *
*******************************************

*******************************************
*       PAGE 4  FRAME SYNC SETUP          *
*FR SYNC   = ON                           *
*MODE      = NORMAL                       *
*MED       = OFF        WINDOW      = 0  *
*SRCH ERRS = 0          CHECK PATTS = 0  *
*LOCK ERRS = 0          LOCK PATTS  = 0  *
*******************************************

*******************************************
*       PAGE 5  ID COUNTER SETUP          *
*COUNT DIR   = UP                         *
*MIN COUNT   = 0       MAX COUNT   = 127 *
*ID WORD LEN = 12      ORIENTATION = MSB *
*  * LOCATION OF LAST ID BIT RECEIVED *   *
*WORD NUMBER = 22      BIT NUMBER  = 15   *
*******************************************

*******************************************
*      PAGE 6  SUBFRAME SYNC SETUP        *
*SF SYNC    = ON                          *
*MODE       = ID                          *
*CHECK ERRS = 0          CHECK PATTS = 0 *
*LOCK ERRS  = 0          LOCK PATTS  = 0 *
*                                         *
*******************************************

*******************************************
*   PAGE 7  FSP ERR ACCUM / DC SETUP      *
*FSP ERR LEN = 1                          *
*DC FORMAT   = HEX                        *
*DC MODE     = MINOR FRM                  *
*WORD #      = 31          FRAME # = 0    *
*DC WORD     =                            *
*******************************************
```

```
*****************************************
*     PAGE 8    TEST PATTERN SETUP      *
*PTTN SELECT = 1                        *
*RATE        = OSC/2                    *
*WORD LEN    = 16       WORDS/FRM = 4096 *
*                                       *
*                                       *
*****************************************

*****************************************
*        PAGE 9   DAC/CAL CONTROL       *
*(DAC)                                  *
*    INPUT FORMAT:BIN   INPUT SHIFT:4   *
*(CAL)                                  *
*    SOURCE:FSC    STEP:1               *
*      MODE:RAMP    POL:POS  VALUE:0     *
*****************************************

*****************************************
*          PAGE 10   DAC SETUP          *
*DAC # : 1                              *
*                                       *
* WORD # : 0      WORD INTERVAL : NONE   *
*FRAME # : 0     FRAME INTERVAL : NONE   *
*                        LOAD  : (ENTER)*
*****************************************

*****************************************
*           PAGE 11  DER SETUP          *
*DER # : 1                              *
*                                       *
* WORD # : 0      WORD INTERVAL : NONE   *
*FRAME # : 0     FRAME INTERVAL : NONE   *
*                         LOAD : (ENTER)*
*****************************************

*****************************************
*     PAGE 12  DR32W INTERFACE SETUP    *
*       DATA XFER = ALWAYS              *
*XFER SAMPLE RATE = FRAME               *
*   INTR 1 SOURCE = FRAME BOUNDARY      *
*INTR 1 = DISABLE      INTR 2 = DISABLE *
*INTERFACE = STANDBY     BUSY = POSITIVE *
*****************************************
```

3.4 LOCAL DISPLAY PAGES

3.4.1 DAC021

The functions associated with the DAC021 are contained on 3 pages numbered Page 9 through 11. Page 9 provides the static setup parameters associated with both the DAC's (Digital to Analog Converters) and DER's (Digital Event Registers). Page 10 is used to select the data source (measurement) for each of the 16 D/A's and page 11 is used to select the data source for each of the three event registers.

3.4.1.1 PAGE 9

```
*************************************************
*          PAGE 9 DAC/DER/CAL CONTROL           *
*                                               *
*   (DAC)                                       *
*   INPUT FORMAT:       INPUT SHIFT:            *
*                                               *
*   (CAL)                                       *
*   SOURCE:         STEP:                       *
*   MODE:           POL:          VALUE:        *
*************************************************
```

FIELD NAME	TYPE	ALLOWABLE VALUES	DESCRIPTION
INPUT FORMAT	STEP	BIN 2's	Binary Two's Complement
INPUT SHIFT	NUMERIC	0 to 10	Number of bits the input data is shifted toward the MSB position (left)
SOURCE	STEP	FSC CAL	Real time data from the frame sync module Calibration data
STEP	STEP	1,2,5,10 & 20	Selects the time period of the Ramp in Secs.
MODE	STEP	RAMP UNIQUE	Selects a 0 to 100% ramp in 10% increments (11 steps). The DER's upper four bits are binarily incremented for each pass through the ramp. Selects a 16-bit data value for calibration.
POL	STEP	POS NEG	DER output data is positive true DER output data is negative true
VALUE	HEXADECIMAL	0 to FFFF	Hexadecimal value used for the unique calibration mode

3.4.1.2 PAGE 10

```
*************************************************
*              DAC SETUP                        *
*                                               *
*    DAC # :                                    *
*                                               *
*    WORD # :       WORD INTERVAL :             *
*    FRAME # :      FRAME INTERVAL :            *
*                     LOAD : (ENTER)            *
*************************************************
```

FIELD NAME	TYPE	ALLOWABLE VALUES	DESCRIPTION
DAC #	NUMERIC	1 to 16	Selects the DAC to be programmed
WORD #	NUMERIC	NONE/	Defines the word number - 0 to location within

			the PCM 65535 format that is to be assigned to the selected D/A. NONE indicates a non-active channel.
WORD	NUMERIC	NONE/	Defines the interval INTERVAL1 to 9999 between the occurrences of supercommutated words. NONE indicates no super-commutation applicable to the selected WORD #.
FRAME #	NUMERIC	NONE/	Defines the frame number 0 to 4095 within the PCM format or that contains the 1 to 4096 selected word number assigned to this D/A channel. NONE indicates that the parameter defined by the word number selected (WORD #) is not subcommutated.
FRAME	NUMERIC	NONE/	Defines the interval INTERVAL1 to 4095 between the occurrences of super-subcommutated words at the frame level. NONE indicates no super-subcommutation applicable at the frame level.
LOAD	FIXED	ENTER	Loads the current information selected for the DAC channel into the memory of the local controller.

3.4.2 CPI012

The CPI012 module's operating parameters are selected on page 12.

```
*********************************************
*        PAGE 12 DR32W INTERFACE SETUP      *
*   DATA XFER =                             *
*   XFER SAMPLE RATE =                      *
*   INTR 1 SOURCE =                         *
*   INTR 1 =                INTR 2 =        *
*   INTERFACE =             BUSY =          *
*********************************************
```

FIELD NAME	TYPE	ALLOWABLE VALUES	DESCRIPTION
DATA XFER	STEP	BOTH NOT SRCH	Transfer data when minor and major syncs are both out of Search.
		BOTH LOCK	Transfer data when minor and major syncs are both in Lock.
		FR NOT SRCH	Transfer data when minor frame sync is out of Search. Major sync state ignored.
		SFR NOT SRCH	Transfer data when major frame sync is out of Search. Minor sync state ignored.
		FR LOCK	Transfer data when minor frame sync is in Lock. Major sync state ignored.
		SFR LOCK	Transfer data when major frame sync is in Lock. Minor frame sync state ignored.
		ALWAYS	Always transfer data - ignore both sync states
XFER SAMPLE	STEP	FRAME	Samples the criteria for RATE data transfer at each minor frame.
		SUBFRAME	Samples the criteria for data transfer at each major frame.
INTR 1	STEP	FRAME BOUNDARY	Generates an interrupt at SOURCE the end of each minor frame.
		SUBFRAME BOUNDARY	Generates an interrupt at the end of each major frame.
INTR 1	STEP	ENABLE	Enables the output of the INTR 1 Source selected.
		DISABLE	Disables the output of INTR 1 regardless of selection.
INTR 2	STEP	ENABLE	Enables the output of an interrupt based on the frame synchronizer losing minor frame Lock
		DISABLE	Disables an output from the source of INTR 2.
INTERFACE	STEP	PRIME	Selects Interface 1 as the output data channel.
		STANDBY	Selects Interface 2 as the output data channel.

BUSY	STEP	POSITIVE	Selects input logic to accept a positive true BUSY signal from the DRB32W interface.
		NEGATIVE	Selects input logic to accept a negative true BUSY signal from the DRB32W interface.

3.5 INTERNAL REGISTERS

3.5.1 DAC021 SETUP REGISTERS

	BIT							
REG #	7	6	5	4	3	2	1	0
	MA/CD							
0	7	6	5	4	3	2	1	0
	MA/CD							
1	15	14	13	12	11	10	9	8
	WD RAM							
2	7	6	5	4	3	2	1	0
	FR RAM							
3	7	6	5	4	3	2	1	0
						SHFT		
4	2'S	LSB	DE+		3	2	1	0
5							CAL	OPR

3.5.1.1 Register 0 and 1

Register 0 and 1 defines the memory address for either the word counter RAM or the frame counter RAM. It is also used to define the calibration data (12 bits (0 - 11) for D/A's and 16 bits (0 - 15) for the event registers).

3.5.1.2 Register 2 and 3

Register 2 is to write or read the data associated with the word count RAM. The data is stored directly in the RAM for a write and fetched directly from RAM for a read. Register 3 operates the same way except for the frame count RAM.

The address that is to be written to or read from is loaded into the ma/cd registers (0,1) and then the appropriate register (2 or 3) is written to or read from. The write register 2 or 3 pulse is the signal used to load the appropriate memory with the data that is placed on the data lines from the IOC module. The read register 2 or 3 pulse is used to gate the memory data back to the IOC data lines.

3.5.1.3 Register 4

The SHFT field determines the number of bits the parallel data from the frame sync will be shifted toward the MSB bit. A 16-bit word is shifted 0 bits while a 12 bit word is shifted left four bits so as to align bit 12 to the MSB of the selected DAC. A maximum of 12 shifts can be supported using this field.

The DE+ bit determines the output polarity of the event registers. A one programmed into this bit will produce positive data at the output of the event registers for positive data input. A zero programmed for the DE+ bit will produce negative true data at the output of the event register for positive data input.

The LSB bit is used to define the orientation of the input parallel data. If the LSB of the parallel data is oriented to bit 0 then the LSB bit has to be programmed to a one. If the MSB bit of the input data is oriented to bit 0 then the LSB bit has to be programmed to a zero. The SHFT field only operates if the data is LSB justified.

The 2's bit is used to change input data that is in a two's complement format to an offset binary format. This bit is functional for either LSB or MSB oriented data.

3.5.1.4 Register 5

The OPR bit controls the loading and reading of the word and frame count memories. If OPR is a zero, the memories can be accessed by the IOC module. If the OPR bit is a one, the memories are accessed by the word and frame counts from the frame sync module. In order to program the memories the IOC module must clear the OPR bit.

The CAL bit is used to enable the user to send calibration data to the D/A's and event registers. This bit is effective in either mode of the OPER bit. The full 16 bits of the MA/CD fields (registers 0 and 1) are used for the event registers while only bits 0 through 11 of the same fields are used to control the D/A's. In the CAL mode all D/A's and event registers are strobed simultaneously.

3.5.1.5 DAC021 Programming Information

The SHFT field determines how many bits the input data will be shifted left so as to align its most significant bit (MSB) with that of the MSB of the DAC. This field is only used for input data that is LSB justified to bit 0.

```
                        DAC DATA ALIGNMENT LSB JUSTIFIED
                        --------------------------------
       M                                  L
       S <--------DAC DATA------------> S
       B                                  B
-------------------------------------------------------------------------
11 10 09 08 07 06 05 04 03 02 01 00
       ---------------------------------
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
-------------------------------------------------------------------------
       M                                                  L
       S <---------------INPUT DATA---------------------> S
       B                   POSITION                       B
                                                                SHIFT
15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00              00
14 13 12 11 10 09 08 07 06 05 04 03 02 01 00                 01
13 12 11 10 09 08 07 06 05 04 03 02 01 00                    02
12 11 10 09 08 07 06 05 04 03 02 01 00                       03
11 10 09 08 07 06 05 04 03 02 01 00                          04
10 09 08 07 06 05 04 03 02 01 00                             05
09 08 07 06 05 04 03 02 01 00                                06
08 07 06 05 04 03 02 01 00                                   07
07 06 05 04 03 02 01 00                                      08
06 05 04 03 02 01 00                                         09
05 04 03 02 01 00                                            10
```

The above diagram shows the relationship of the input data word, its length and shift requirement to align its MSB to the MSB of the DAC. A 16 bit input word would not require any shifting whereas an 8 bit input word would require an 8 bit shift so that bit 7 would be aligned to the DAC MSB (bit 11). In this case the higher the bit number the more significant the digit.

If the input data word has its MSB justified to the LSB position then no shifting is required since the LSB position of the input is connected to the MSB of the DAC as shown below. In this case the lower the bit number the more significant the digit.

This realignment is accomplished in the DAC input circuitry by not selecting the LSB JUSTIFY setup parameter bit. The LSB position of the input path is automatically connected to the MSB input to the DAC and so on down to the last of the 12 bits which drive the DAC. Therefore, regardless of the input data word length the alignment to the DAC is automatically supported. The insignificant bit positions in either case are cleared to zero by the serial to parallel conversion circuitry of the FSC module or the shift circuitry of the DAC module.

The LSB bit is used by the operator to identify to the DAC module that the input data is LSB justified. LSB justified is defined as the LSB of the input word being aligned at bit position zero of the input path. If the data being input from the FSC module is LSB justified then the SHFT field is active and performs the selected shift of data to align its MSB with that of the DAC's MSB input. If this bit is not set, the DAC assumes the data input from the FSC module has had its MSB aligned to the LSB position of the input path and performs a realignment of this data to the DAC. In this case no shifting is necessary.

The 2's bit defines the input data format to the DAC. If the bit is set, the input data is considered to be two's complement. If the bit is not set, the input data is considered to be offset binary (for bipolar DAC outputs) or straight binary (for unipolar DAC outputs).

The DE+ bit enables the user to select the output polarity of the Digit Event (DE) registers. If DE+ is set, the output from the three event registers will be positive true for a positive input. If the DE+ bit is not set, the output from the three event registers will be negative true for a positive input. The outputs from the event registers are all TTL levels.

The OPR bit is set to enable the DAC module to process the input data from the FSC module. The OPR bit is not set when the Word and Frame RAM's are to be programmed (word/frame/ interval assignment to DAC and DE selections). Only the word and frame RAM's are controlled by this bit. The other register bits can be altered regardless of the state of this bit.

CALIBRATION

The CAL bit controls the input data source of the DAC's and DE's. If this bit is set, the input data is derived from the selected calibration mode. If the bit is not set, the input data source is derived from the output of the FSC module (real time).

There are two calibration modes associated with the DAC module, "UNIQUE and RAMP". Unique mode enables the user to select a particular value to be sent to the DAC's and DE's. Ramp mode selects dynamic, predetermined data values for the DAC's and DE's at selectable rates.

The user selects the desired value (from 0000 to FFFF (hexadecimal)). This field is only valid during the unique mode. The value selected by the user is loaded into the first two setup registers. The loading of the second register causes the module to generate the appropriate strobe to all DAC's and DER's.

The user can select 1, 2, 5, 10 or 20 seconds of dwell for the ramp mode. The step value selected determines the amount of time it will take to traverse the 65536 (0000 to FFFF) values of the ramp. The STEP field is not active in the UNIQUE mode.

MODE = UNIQUE
VALUE = 0 TO FFFF - The user can select a hexadecimal value between 0 and FFFF. The total value selected will be sent to the DE registers while only the lower 3 hexadecimal digits will be sent to the DAC's (bit 11 - MSB, bit 0 - LSB).

MODE = RAMP
STEP = 1,2,5,10,20 - The hexadecimal ramp will output values from 0 to FFFF in increments of 1. The time to increment from 0 to FFFF is determined by the time step selected. Obviously the time to go from 0 to FFF will be 1/16th that of the selected time step. For a one second step the DE register will cycle from 0 to FFFF while the DAC will ramp from its lowest to highest value sixteen times.

3.5.2 CPI012 SETUP REGISTERS

REG #	BIT 7	6	5	4	3	2	1	0	
0	BUS NEG	ATTN 2 EN	ATTN 1 EN	ATTN1 SRCE	SMPL XFER	XFER 2^2	XFER 2^1	XFER 2^0	Read/ Write Register
1	SELECT CHANNEL 1 AS PRIME								Write only Register
2	SELECT CHANNEL 2 AS PRIME								Write only Register
1							CH2 PRM	CH1 PRM	Read only (Status) Register

3.5.2.1 Register 0

The XFER field selects the synchronizer status that will determine when the interface begins transferring data. The decoding of these bits are as follows.

2^2	2^1	2^0	FUNCTION
0	0	0	Both not in search
0	0	1	Both in lock
0	1	0	Frame not in search
0	1	1	Subframe not in search
1	0	0	Frame in lock
1	0	1	Subframe in lock
1	1	0	Always transfer
1	1	1	Not used

The SMPL XFER bit determines when the transfer criteria above is sampled. A one will sample the transfer status on the minor frame boundary (at the end of each frame). A zero will sample the transfer status on the major frame boundary (at the end of the subframe).

The ATTN 1 SRCE bit selects which boundary condition (frame or subframe will cause an interrupt to be generated. A one will select the end of the minor frame as the source. A zero will select the end of the subframe as the source.

The ATTN 1 EN bit enables the generation of an interrupt on the boundary conditions selected above when set to a one. A zero disables this interrupt.

The ATTN 2 EN bit enables the generation of an interrupt on the loss of minor frame lock when set to a one. A zero disables this function.

The BUSY NEG bit enables the interface's BUSY signal to be either positive true or negative true. A one enables a negative true input BUSY signal to accepted by the interface module. A zero enables a positive true input BUSY signal to be accepted by the interface module. Normally the DRV11 interface outputs a negative true signal while the DR32W typically outputs a positive true signal although the DR32W does have an on-board polarity selection for the busy signal.

3.5.2.2 Register 1 and 2

Register 1 and 2, in the write mode, enable the user to select which one of the two DRB32W interfaces will be active. Issuing a write register 1 will cause the CPI012 to set Channel 1 to the PRIME or active channel. Issuing a write register 2 will cause the CPI012 to set Channel 2 as the PRIME channel. Whichever channel is not set to prime is considered to be in the STANDBY mode. The writing of register 1 or 2 is accomplished by decoding the address lines and does not depend on the data bits.

Register 1 is provided with a read-back capability that can be used to determine which of the two output channels is active. Bit 0 signifies channel 1 is active while bit 1 indicates that channel 2 is active. Reading back a logic high state indicates that the particular channel is active (PRIME).

3.5.2.3 DRB32W Interface Operation

The Model 3440 Frame Synchronizer being supplied to GE contains an interface that permits it to transfer data to a DEC computer provided with a DRB32W interface module. The Model 3440 interface is provided with a 1K word FIFO that acts as a buffer between the Model 3440 and the computer. Data is written to this buffer based on two selectable parameters, one is the first word to be transferred and the second is the level of synchronization achieved before transfers begin.

The first word transferred can be the first word of a minor frame or the first word of a major frame. The level of synchronization is determined from the minor frame synchronizer and the major frame synchronizer (subframe). If the format only contains a minor frame then the first word transferred should be the first word of the minor frame and the level of synchronization should be frame Lock. If the format contains a subframe then the first word transferred should be the first word of the major frame and the level of synchronization should be frame and subframe Lock.

When the above conditions are selected and become active, the FIFO will begin to accept data. If the interface (DRB32W) is not programmed and ready prior to the above conditions becoming active, the user runs the risk of the FIFO becoming full. Once the FIFO becomes full, the 3440 interface halts transfer operation and cannot be resumed without initialization (reset).

The 3440 interface provides an interrupt (ATTN) to the DRB32W as well as three status bits (STATUS A, B, C). An interrupt can be generated which indicates two conditions. The first condition will generate an interrupt when the frame synchronizer loses minor frame

synchronization (Lock) and reverts to the Search mode. The second condition is when the end of the minor frame or the major frame has occurred. The second condition is selectable (either minor or major frame) through the 3440's interface setup parameters. Each of these conditions can be independently disabled via the setup parameters. If both are disabled there will be no interrupt generated.

The three status bits indicate the following conditions. STATUS A, when set indicates that the FIFO is full. STATUS B, when set indicates that the frame synchronizer is in the Lock Mode while STATUS C, when set indicates that the subframe synchronizer is in the Lock Mode.

The DRB32W interface presents to the 3440 interface two initialization (reset) signals that will cause the 3440 output interface to be placed in an initialized state (note: FIFO will be reset). These two signals are labeled INIT and FUNCT 2. The generation of either of these signals will cause the output interface to be re-synchronized to the data format output from the frame/subframe synchronizer module. When these signals are generated care must be exercised to insure that the DRB32W interface card is also initialized and ready for data to be re-transmitted from the Model 3440.

The correct transfer of data depends on the order in which programmable parameters are loaded and activated. The setup parameters associated with the frame sync, the D/A converter and the interface should all be programmed first except the bit that "turns - on" the frame sync function. The DRB32W interface module should then be programmed next. The last parameter to be activated is the frame sync "turn - on" bit. This will ensure that after the frame sync achieves the proper synchronization state, data will be transferred to the computer in the correct sequence and the DRB32W interface will be ready to accept the data.

3.6 REMOTE CONTROL (IEEE-488)

3.6.1 DAC021

DAC SETUP	PID	PAR
input format	FMT	1 character 0 = BINARY 1 = 2's complement
input shift	SFT	XX range = 00 - 10
source	SOU	1 character 0 = FSC 1 = CAL
step	STP	1 character 0 = 1 1 = 2 2 = 5 3 = 10 4 = 20
value	VAL	XXXX range = 0000 - FFFF
mode	MOD	1 character 0 = RAMP 1 = UNIQUE
output polarity	OPL	1 character 1 = POSITIVE 0 = NEGATIVE

DAC SETUP	PID	PAR
dac number	DAC	XX range = 01 - 16
word number	AWN	XXXXX range = 00000 - 65535, or the word "NONE "
word interval	AWI	XXXX range = 0001 - 9999, or the word "NONE"
frame number	AFN	XXXX range = 0000 - 4095, or the word "NONE"
frame interval	AFI	XXXX range = 0001 - 9999, or the word "NONE"
load	ALD	1 character L = LOAD

DER Setup	PID	PAR
der number	DER	X range = 1 - 3
word number	EWN	XXXXX range = 00000 - 65535, or the word "NONE "
word interval	EWI	XXXX range = 0001 - 9999, or the word "NONE"
frame number	EFN	XXXX range = 0000 - 4095, or the word "NONE"
frame interval	EFI	XXXX range = 0001 - 9999, or the word "NONE"
load	ELD	1 character L = LOAD

3.6.2 CPI012

DRB32W Interface	PID	PAR
data transfer	XFR	1 character 0 = BOTH NOT SRCH 1 = BOTH LOCK 2 = FR NOT SRCH 3 = SFR NOT SRCH 4 = FR LOCK 5 = SFR LOCK 6 = ALWAYS
sample rate	SRT	1 character 1 = FRAME 0 = SUBFRAME
intr 1 src	INS	1 character 1 = FRAME BOUNDARY 0 = SUBFRAME BOUNDARY
intr 1 enable	INO	1 character 0 = DISABLE 1 = ENABLE
intr 2 enable	INT	1 character 0 = DISABLE 1 = ENABLE
prime channel	PCH	1 character 1 = 1 2 = 2
busy	BSY	1 character 0 = POSITIVE 1 = NEGATIVE

3.7 DAC OUTPUT VOLTAGE RANGE SELECTION

The output range of the D/A converters can be individually selected by placing the 5 DIP switches in one of the following 5 sequences for each of the 16 D/A converters located on the DAC021 module.

VOLTAGE RANGE	SW POS 1	SW POS 2	SW POS 3	SW POS 4	SW POS 5
± 10.0	OPEN	CLOSE	OPEN	CLOSE	OPEN ***
± 5.0	OPEN	CLOSE	OPEN	OPEN	CLOSE
± 2.5	OPEN	CLOSE	CLOSE	OPEN	CLOSE
0 to +10.0	CLOSE	OPEN	OPEN	OPEN	CLOSE
0 to +5.0	CLOSE	OPEN	CLOSE	OPEN	OPEN

*** Represents factory setting.

Section 4
THEORY OF OPERATION

4.0 INTRODUCTION

This section contains a detailed description of the circuitry that constitutes the DACO21 and the CPIO12. The schematics for each of these modules are contained in Section 5. The information presented here provides the user with a deeper understanding of the operation of the module and is accomplished through a page by page description of the schematics (logic diagrams).

All schematics flow from left to right, ie. the inputs are on the left while the outputs are on the right. Each input to a page is labeled as to its name and the page from which it was generated. Each output is labeled with a name and to which page it is sent. All logic elements are identified as to the type of part (74LS240) and their location on the module (U14). Each part on the modules are allocated a reference designation by which it can be located in the its schematics, assembly drawing and parts list. Also each of the schematic sheets is identified as to the function it performs.

4.1 DACO21

4.1.1 LOGIC SHEET 1

Sheet 1 defines the interconnection of the D/A and DER outputs with the P1 connector. The 16 D/A's are output on A1 through A32. DER 1 is output on the B pins of connector P1 and DER 2 is output on the C pins of connector P1. DER 3 is split between the B and C pins of connector P1.

4.1.2 LOGIC SHEET 2

The setup bus signals from the Model 3440 controller are brought in on this connector (P2). The signals consist of 8 address, 8 data and 4 control lines.

4.1.3 LOGIC SHEET 3

Logic Sheet 3 consists of the signals that interface the frame synchronizer with the DACO21 Module. The signals consist of 16 data lines and 11 control lines. The word and frame count values are used to address the distribution RAM's.

4.1.4 LOGIC SHEET 4

This sheet contains the setup bus address decoding and control signal generation used to write and read the setup registers on the DACO21 module. The 8 address lines are buffered by IC U6 and the upper 5 lines are sent to exclusive OR gates U83 and U82 where the bus address lines are compared against the selected module address determined by DIP switch SW1. The lower 3 address lines are routed to the write and read register decoders U16 and U17 respectively.

Control signals R/W, STB, SCLK and ACK are buffered by IC U5 and act as the interface between the unit setup bus and the module logic. The SYB signal is delayed by shift register U38 and gated by U69 to produce a properly oriented write pulse. This pulse in conjunction with module enable (DACEN) and the R/W line are used by decoder U16 to produce the 6 write register strobes (WR 0 through WR 5). IC U17 generates the read register strobes used to enable the controller to read the information contained in the 6 setup registers. Sheet 4 also contains the resistor pullups for the rest of the module.

4.1.5 LOGIC SHEET 52

Logic Sheet 5 shows the setup registers and buffers that control the DACO21. Registers 0 and 1 (U37 and U21)represent the addresses for the WORD and FRAME RAM's. These two registers are also used to hold the calibration data. Buffer (U64) is used to pass the setup bus data between the controller and the internal setup data bus of the DACO21. Buffers U43 and U32 direct the pathway of the internal setup bus data to and from the WORD and FRAME RAM's. IC U15 is a static register that contains the operational setup parameters of the DACO21. IC U26 represents register 5 and only contains the OPER and CAL control bits.

4.1.6 LOGIC SHEET 6

IC's U7 and U18 are 8 bit registers that store the parallel PCM data from the frame sync. The stored PCM data is routed to multiplexer's U50, U28 and U61 where the control bit LSB JUSTIFY selects between shifted and unshifted data. The unshifted data (CLKPD 0 - 11) is oriented such that bit 0 is the MSB and bit 11 is the LSB and represents one of the inputs to the multiplexer. The other input is the parallel data that has been processed by the DAC shifter (SDATA 0 - 11) where bit 0 is the LSB and bit 11 is the MSB. The output of this multiplexer is sent to inverting buffers U71 and U60. The data sent to the DAC's requires inversion due to the input requirements of the D/A chip. The control line for these buffers enables them when the DACO21 is not in the CALIBRATION mode. The other set of inversion buffers U60 and U68 accept the calibration data that is stored in registers 0 and 1 (bits 0 through 11) and enable it on the DAC data lines when the DACO21 is placed in the CALIBRATION mode. The outputs from these buffers are connected to all of the D/A converter chips on the module. Gate U82 pins 4, 5 and 6 is used to handle input data that is in 2's complement format. The exclusive OR gate inverts the MSB of the real time data going to the DAC's if the input data is 2's complement. If the data is offset binary it passes the MSB unaltered.

4.1.7 LOGIC SHEET 7

Logic Sheet 7 represents the first portion of the DAC data shifter. These 12 IC's support the shifting from 0 to 7 bits. A 0 shift is accomplished by applying a binary value of 7 to each of the IC's. A shift of 7 bits (input bit 8 would be output on line FSFT 11) is performed by changing the control value of the IC's to a binary 0. The shift control lines SADR0 to SADR2 are generated by a PROM on sheet 9. The IC 74LS244 is a buffer that enables the applied control signals (CAL and OPER) to drive the additional inputs required by the design.

4.1.8 LOGIC SHEET 8

This sheet controls the remaining four bits of shift that can be supported by the DACO21. The total number of bits that can be shifted by this logic is 10 (input data can be shifted from 0 through 10 bits) and is selected by the operator through the SHFT field of setup register 4. SADR3 and SADR4 are the control lines for the bit shifting on this sheet. The output from the shifter is labeled SDATA 0 through SDATA 11 and is applied to the multiplexer on sheet 6.

4.1.9 LOGIC SHEET 9

The logic on sheet 9 generates the data lies used to drive the event registers of the DACO21 module. The data sent to the DER's is labeled DEDATA0 through DEDATA15. In the CALIBRATE mode IC's U45 and U46 enable the data stored in registers 0 and 1 to be placed on the DER lines. In the non-calibrate mode gates U79 pin 3 and 6 control which set of two buffers are enabled onto the DER lines. If the DE+ bit is set then IC's U57 and U59 are enabled. This places positive true data onto the DER lines. For DE+ not true IC's U58 and

U47 are enabled. These IC's are inverting, hence the real time data from the frame sync will be inverted and present a negative true output for the Digital Event registers. The shift control PROM is shown at the bottom of the page. This IC converts the shift value the user inputs to one which will produce the desired number of shifts through the DAC shifter on sheets 7 and 8.

4.1.10 LOGIC SHEET 10

U8 and U9 store the input word count value received from the frame sync. It is only output to the RAM when the module is in the OPERATE mode and acts as the real time address for the WORD RAM. IC's U19 and U20 buffer the setup address path to the WORD RAM (U30 and U41) for a read or write and can only be enabled when the module is not in the OPERATE mode. Setup buffer U43 (WORD RAM data on sheet 5) supplies the data to the WORD RAM and gate U79-8 provides the write pulse.

The output from the WORD RAM is sent to sheet 5 (setup read and write) and sheet 12 (real time). The lower four bits of the WORD RAM are buffered by U54 and applied to the FRAME RAM as the upper four address lines.

4.1.11 LOGIC SHEET 11

The operation of the FRAME RAM shown on this sheet is the same as that of the WORD RAM from sheet 10 except that the upper four address bits for real time operation are derived from the output of the WORD RAM. The lower 12 address lines (real time) are driven by the frame count value received from the frame sync module. The setup data for this RAM is buffered through U32 on sheet 5.

4.1.12 LOGIC SHEET 12

This sheet generates the individual strobes for all of the D/A and DER data registers. Real time strobes are derived from the output of either the WORD or FRAME RAM as selected by U42 and U31. The selection criteria is the logic state of bit 7 of the WORD RAM which if it is a logic one will select the FRAME RAM output and conversely a logic zero selects the output from the WORD RAM. The selected output represents the D/A or DER to which the current real time data word is to be sent. The selected output is a binary number from 0 to 19 which is decoded by IC's U55, U76 and U67. A value of zero indicates that the current data word is not to be sent to any of the D/A's or DER's. A value from 1 to 16 defines one of the 16 available D/A converters. A value of 17 through 19 defines the three DER's on the DAC021. The value that is stored in either the WORD or FRAME RAM is determined by the user when he defines the word distributions for his PCM format.

IC U52 is used to delay the real time strobe from the frame sync so that the delays in the shifter and RAM are accounted for. The output from this chip drives the DAC and DER address decoders which produces a data strobe if the current word has been programmed for distribution to a DAC or DER.

IC's U66, U56, U90, U89 and U77 select between the real time DAC and DER strobes and the CALIBRATION mode strobe generated by delaying the write register 1 (WR 1) strobe in shift register U81. The delayed write strobe is applied to all of the DAC's and DER's by connecting all of the selection multiplexer's "B" inputs together.

4.1.13 LOGIC SHEETS 13 THROUGH 20

These sheets contain the data registers and D/A converter IC's. The DDATA is applied to all of the D/A converter registers. An appropriately generated D/A strobe will cause the DDATA to be stored into the holding registers (U103 and U108 for DAC 1 if DAC STB 1 is active). The resultant data output from the registers drives the D/A converter chip and converts the

digital input to an equivalent analog output. Each of the D/A converter chips is supplied with a 5 position DIP switch that determines its output voltage range. The switch positions are given in section three of this manual. Each of the sheets referenced here show two DAC's.

4.1.14 LOGIC SHEETS 21 AND 22

These two sheets contain the three digital event registers and their output buffers. Each of the DER's is provided with 16 bits of storage via two 8 bit wide registers that are strobed when the user has assigned a data word to be them (U23 and U24 represent DER #1's storage register while U34 and U35 represent the output buffers).

4.2 CPI012

4.2.1 LOGIC SHEET 1

Logic sheet 1 consists of the input and output signal designations for connector P1 of the CPI012 module. Connector P1 provides the outputs to the two DRB32 interfaces in the DEC computer. All signals designated as 1- represent the connections to the first interface (J11 and J12 on the rear panel) and those designated as 2- for the second interface (J13 and J14 on the rear panel). The signals located on P1 - C26/27, C28/29 and C31/32 represent the rear panel status signals FR LOCK(-) (J7), FRM CLK(-) (J5) and SFRM CLK(-) (J6) respectively.

4.2.2 LOGIC SHEET 2

The P2 connector shown represents the internal setup bus of the Model 3440 and consists of 8 Data, 8 Address and 4 Control lines (R/W(-), STB(-), SCLK(-) and ACK(-)).

4.2.3 LOGIC SHEET 3

Logic sheet 3 consists of the interface signals from the frame synchronizer module within the Model 3440. They consist of the parallel data (16 bits) as well as control and status signals. These signals are input through connector P3.

4.2.4 LOGIC SHEET 4

Logic sheet 4 contains the address decoding associated with the writing and reading of the setup registers for the CPI012 module. The 8 address lines are buffered by U4 and the upper 5 address bits are decoded through the exclusive OR gates U3 and U5. The other inputs to the exclusive OR gates are derived from DIP switches which are set at the factory to correspond to the module address (each module in the unit is assigned a different address). The outputs of the exclusive OR gates are AND'ed to produce the module enable signal that indicates the card is being address by the unit controller.

The three control lines (R/W(-), STB(-) and SCLK(-)) are buffered by U6. The STB(-) signal is delayed through the shift register U15. Its outputs (pins 3 and 5) are applied to gate U17 to generate an appropriate write strobe used by register decoder U14. The write strobes from U14 are applied to the setup registers on sheet 5 which hold the operating parameters of the CPI012. Pin 6 of U15 is used in conjunction with the R/W(-) line to generate and acknowledge signal back to the controller when a read register is requested. IC U7 generates the read control signals for the setup registers.

4.2.5 LOGIC SHEET 5

The one setup register U31 is located on sheet 5 and is driven by bi- directional buffer U32. U32 controls which direction the data from the setup bus is routed. When the R/W(-) line is low the data is passed from the controller to the CPI012 module for the purpose of writing it to the registers and when it is high the data is read back from the register to the setup controller. U31 is designated register 0 and is loaded by WR 0(-) and read by RR 0(-). Writing to register 1 and 2 determine the mode of the module with reference to the PRIME and STANDBY ports of the CPI012. A write to register 1 enables channel 1 to be PRIME while a write to register 2 enables channel 2 to be PRIME. The channel that is not PRIME is considered to be the STANDBY channel. U12 is a flip-flop that stores the current state of the output channels to the DRB32's. The state of the active channel can be read from the local or remote controller by performing a read of register 1. A read of register 1 is controlled by signal RR 1(-) applied to U30.

U1 converts the single ended status signals (FR PULSE(-), SFR PULSE(-) and LFLOCK(+)) to differential signals for output to the rear panel. R1 is set of 15, 1Kohm pull-up resistors used by the module to tie off the critical inputs of certain IC's.

4.2.6 LOGIC SHEET 6

Sheet 6 generates the signal that enables the on-board FIFO's to begin filling with data. The enable signal (FWR ENAB (-)) is controlled by the selection of the transfer status state of the frame synchronizer. It is also dependent on the selection of where the buffer will start, the beginning of a minor or major frame.

U33 is used to determine whether the frame synchronizer has reached the proper status state by using the XFER bits to select the frame synchronizer status state. U34 is used to select either the frame or subframe pulse to sample the selected status state of the frame synchronizer. If the frame synchronizer has attained the selected state then the FIFO's are enabled to start storing data. The remaining circuits on this sheet guarantee that the first word to be stored is actually the first word of the minor or major frame. This circuitry also guarantees that the last word of the minor frame will be stored when the frame synchronizer loses its current status state.

4.2.7 LOGIC SHEET 7

The logic on this sheet determines the timing between the CPI012 and the DRB32 interface. The top half of the sheet is used to generate the FIFO write pulse and determine if the FIFO is full. If the FIFO becomes full, the circuitry halts all further FIFO writes until the CPI012 and the DRB32 is re-initialized. U23 and U24-9 provide the proper delay between the input data strobe (WRD STR +1(+) and the time the FIFO write pulse (FIFO WR(-)) is generated so that the data input to the FIFO's has stabilized.

The bottom half of the logic is used in synchronizing the CPI012 timing to that of the DRB32. In order to start transferring data to the DRB32, the FIFO must not be empty (EMPTY(-) is high), the DRB32 interface must be ready (READY (+) is high) and there are no pending interrupts (PRE ATTN(-) is high). When these three conditions are met a FIFO read (FIFO RD(-)) signal is generated to read the data from the FIFO and is then delayed by U35 and U36 to produce the Cycle Request signal to the DRB32 interface. When the DRB32 interface responds with a Busy signal, the CPI012 terminates the current FIFO read and the Cycle Request. If the FIFO is empty when the DRB32 responds with its Busy signal, the circuitry (U44-6) stores this fact and disables further transfers from taking place until the FIFO has accepted more data from the frame synchronizer.

4.2.8 LOGIC SHEET 8

Logic sheet 8 contains the data FIFO's that smooth the transfer of data between the frame synchronizer and the DRB32 interface. The data presented to the FIFO's (U8 and U9) is loaded by FIFO WR(-). When the first word is loaded into the FIFO's, the empty signal goes high and assuming the DRB32 is ready and no interrupts are pending a FIFO RD(-) signal will be generated which will enable the output of the FIFO's to be applied to latches U39 and U49. When the DRB32 interface responds with a Busy signal, it is used to latch the data from the FIFO's into U39 and U49. The Busy signal also terminates the FIFO read and maintains the data in the latches as long as it is active.

The CPIO12 has interrupt capability and is determined by the logic on this sheet. An interrupt can be generated when the frame synchronizer loses frame lock or when the end of a minor or major frame has been detected. Both sources of interrupt can be active, ie. an end of minor frame as well as loss of lock can generate the interrupt. The interrupt from the end of the minor or major frame is normally used to signify to the computer that a buffer has been completely transferred. The selection of minor or major frame generation of the interrupt is controlled by U37 through signal SEL ATTN 1(+). With SEL ATTN 1(+) low the minor frame is active and with it high the major frame is active. An enable signal is provided through ATTN1 EN(-).

The second source of interrupt, frame lock loss is enabled by signal ATTN2 EN(-) at gate U48-3. Either of the interrupts are passed by gate U48-10 if they are active. Flip-flops U47-5 and U47-8 are used to store the fact that an interrupt from either source has become active. The PRE ATTN(-) signal is used to halt transfers of data to the DRB32 interface until the interrupt generate by ATTN(+) has been serviced by the computer. The interrupt service routine of the computer will de- activate the DRB32 interface which in turn will cause READY(-) to go high and clear the PRE ATTN and ATTN flip-flops. If both interrupts are active, the computer can determine which one has caused the interrupt by reading the state of the STATUS B line on the DRB32 interface.

4.2.9 LOGIC SHEET 9

Sheet 9 provides the output of pertinent signals depending on which of the two channels has been selected to be the PRIME output. IC U20 selects the appropriate source of control signals from the DRB32 interface that has been chosen as PRIME. The gates of U42 determine which port's output control signals will be active based on the selection of the PRIME channel.

4.2.10 LOGIC SHEETS 10 AND 11

These logic sheets provide the buffers for the signals that are output to the two DRB32 interfaces. Sheet 10 is for channel 1 and sheet 11 is for channel 2. The selection of the PRIME channel determines which of these groups of logic will be enabled.

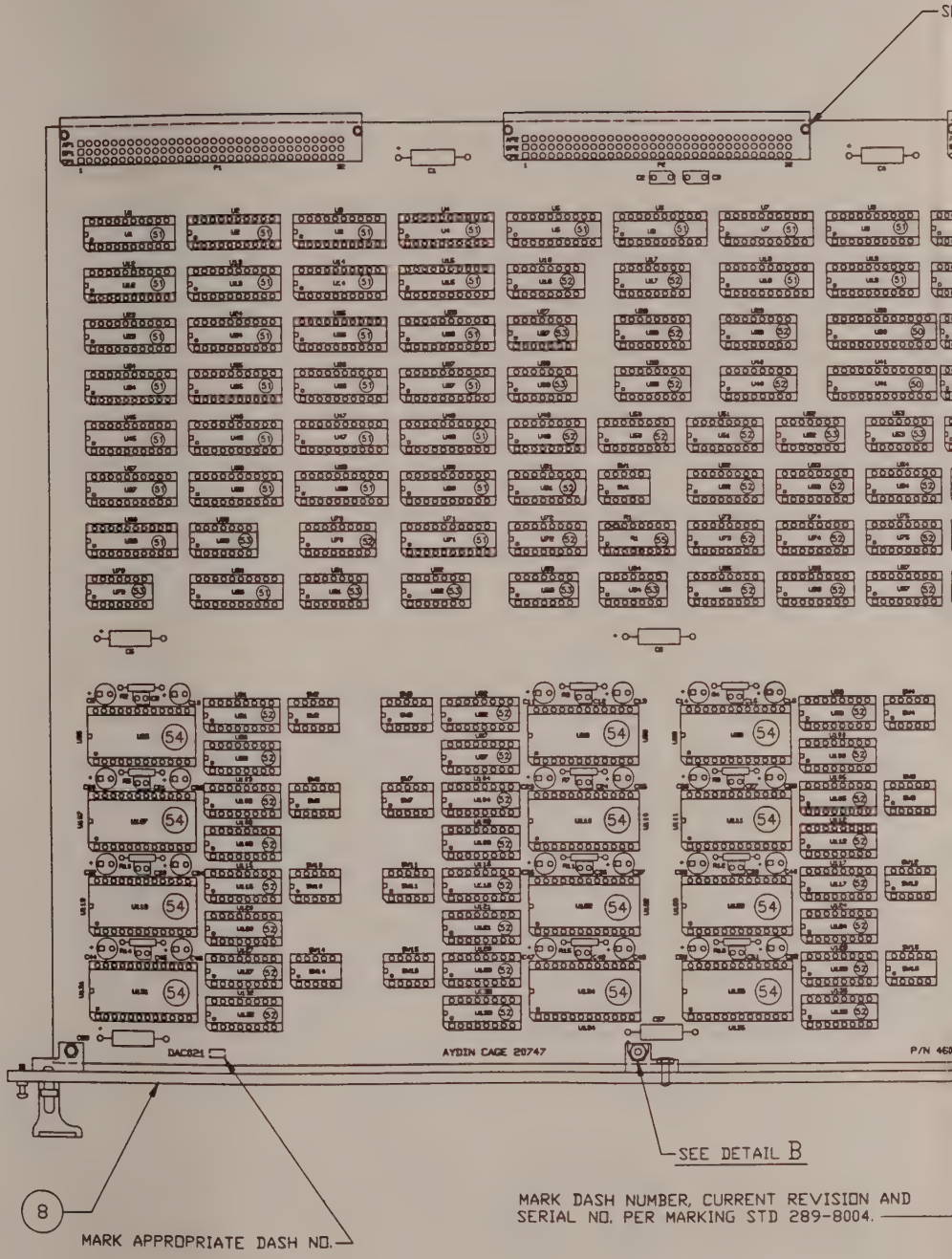
Section 5
DRAWINGS

5.0 INTRODUCTION

This section consists of the drawings that define the DAC021 and the CPI012 modules. They are presented in the following order.

DESCRIPTION	NUMBER
DAC021 Assembly Drawing and Parts List	460-2281-501
DAC021 Logic Diagram	500-0989
CPI012 Assembly Drawing and Parts List	460-2255-501
CPI012 Logic Diagram	500-0988

...INS PROPRIETARY AND CONFI-
...FORMATION OF THE COMPANY, AND IS
...ERED ON THE EXPRESS CONDITION THAT IT IS
...T TO BE DISCLOSED OR REPRODUCED IN WHOLE OR
PART, NOR USED FOR MANUFACTURE BY ANYONE
OTHER THAN THE AYDIN CORPORATION; AND THAT NO
RIGHT IS GRANTED TO DISCLOSE OR SO USE ANY
INFORMATION CONTAINED IN THIS DOCUMENT.



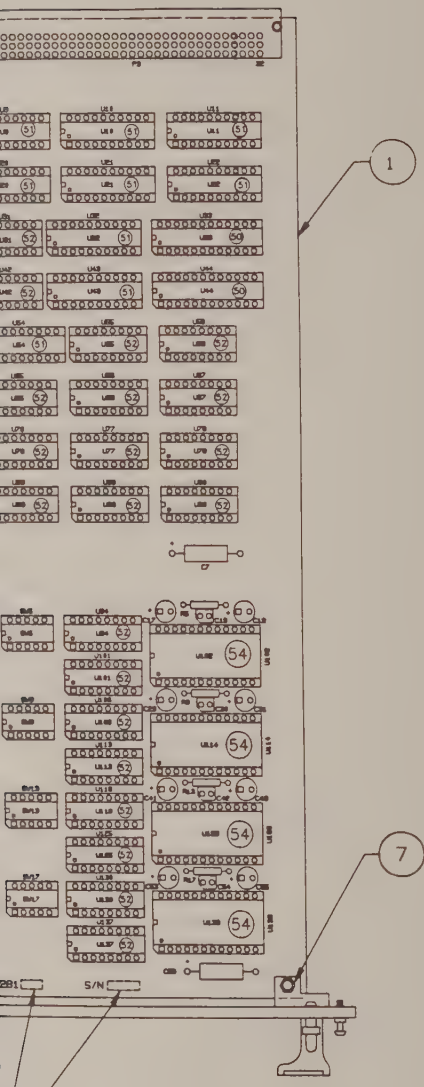
NOTES:

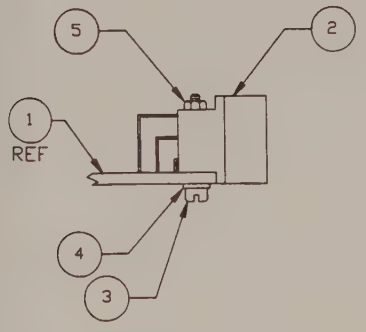
1. FOR GENERAL MANUFACTURING NOTES SEE DWG. NO. A)285-8057.
2. THE MAXIMUM COMPONENT PROFILE IS .450.

4	3	2	1

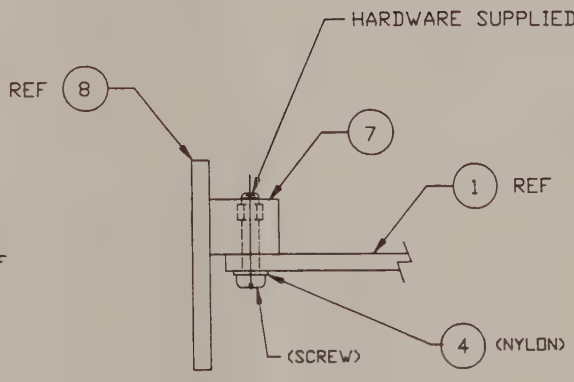
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	–	RELEASED	4-3-91	

DETAIL A





DETAIL A
SCALE 2:1



DETAIL B
SCALE 2:1

SEE SEPARATE PARTS LIST PL460-2281-501

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND APPLY BEFORE FINISH SURFACE ROUGHNESS 125
TOLERANCE ON
FRACTIONS ± 1/64 | DECIMALS .XX=.02 ± .XXX=.005 | ANGLES ± 1/2°
MATERIAL —
FINISH —
NEXT ASSY | USED ON
APPLICATION

DRAWN	J. Hallman	4-1-91
CHECKED	Ken Weaver	4-2-91
DRAFTING		4-4-91
ENGINEER		4-3-91
APPROVED MFG	Y. Polsky	4-7-91
APPROVED QA	Dan Mueller	4-2-91

AYDIN COMPUTER AND MONITOR Division
700 DRESHER ROAD HORSHAM, PA 19044

CARD ASSEMBLY
DACØ21-1

SIZE	CAGE NO.		REV
D	20747	AD460-2281-501	–
SCALE —		SHEET 1 OF 1	

DAC.S00
COVER SHEET

DAC.S01
P1 CONNECTOR

DAC.S05
DAC SETUP REGISTERS

DAC.S06
DAC DATA GENERATION

DAC.S10
WORD COUNT RAM

DAC.S11
FRAME COUNT RAM

DAC.S15
DAC 5 & 6 OUTPUTS

DAC.S16
DAC 7 & 8 OUTPUTS

DAC.S20
DAC 15 & 16 OUTPUTS

DAC.S21
DER 1 & 2 OUTPUTS

SHEET	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
REV.															
SHEET	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45
REV.															
SHEET	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
REV.	—	—	—	—	—	—	—								
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
REV.	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	—	RELEASED	1-28-91	

2 CONNECTOR

DAC.S03
P3 CONNECTOR

DAC.S04
ADDRESS DECODE
AND
READ/WRITE STROBES

IRST STAGE
OF
C DATA SHIFT

DAC.S08
SECOND STAGE
OF
DAC DATA SHIFT

DAC.S09
DE DATA GENERATION
SHIFT ADDRESS GENERATION

C AND DE STB
GENERATION

DAC.S13
DAC 1 & 2 OUTPUTS

DAC.S14
DAC 3 & 4 OUTPUTS

9 & 10 OUTPUTS

DAC021.S18
DAC 11 & 12 OUTPUTS

DAC.S19
DAC 13 & 14 OUTPUTS

DER 3 OUTPUTS

6197	
NEXT ASSY.	USED ON
APPLICATION	

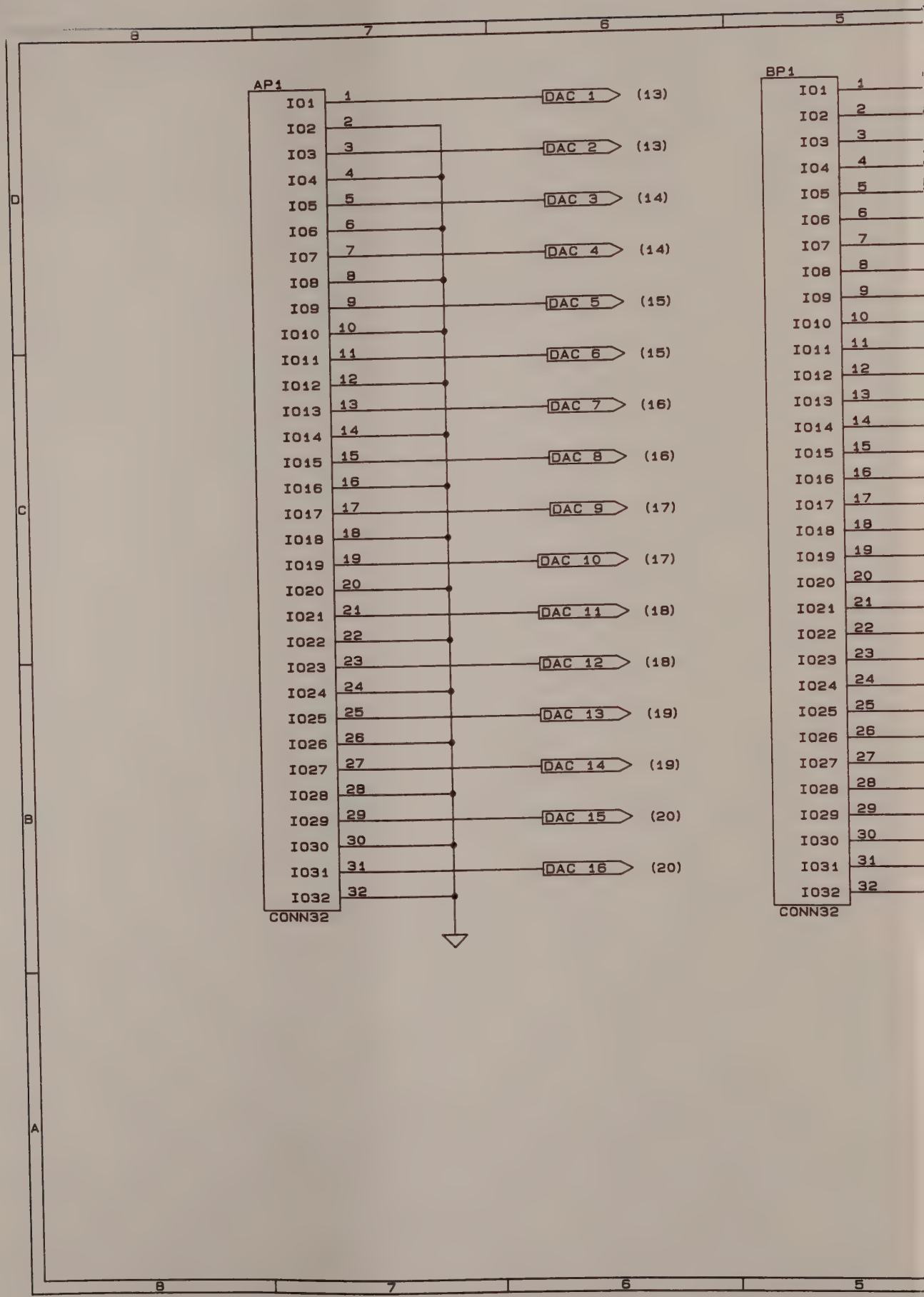
DRAWN E HOLTZ	DATE 9/12/90
CHECKED	28JAN91
DRAFTING	28JAN91
ENGINEER E HOLTZ	9/12/90
APPROVED	1/28/91
MAGNETIC MEDIA	

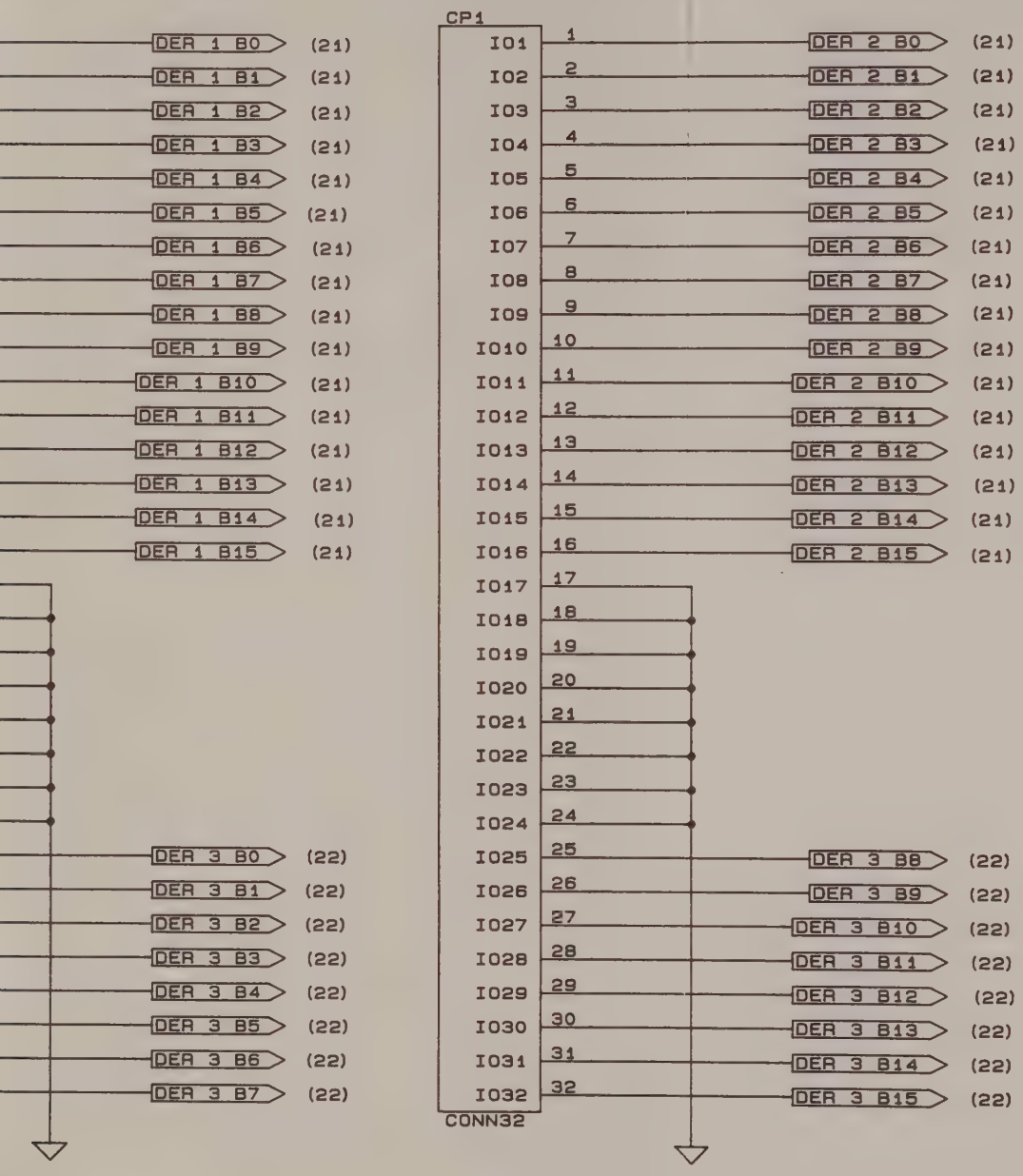
AYDIN COMPUTER AND MONITOR DIVISION
700 DRESHER ROAD
HORSHAM, PA 19044

LOGIC DIAGRAMS
FOR
DAC021 D/A CONVERTER

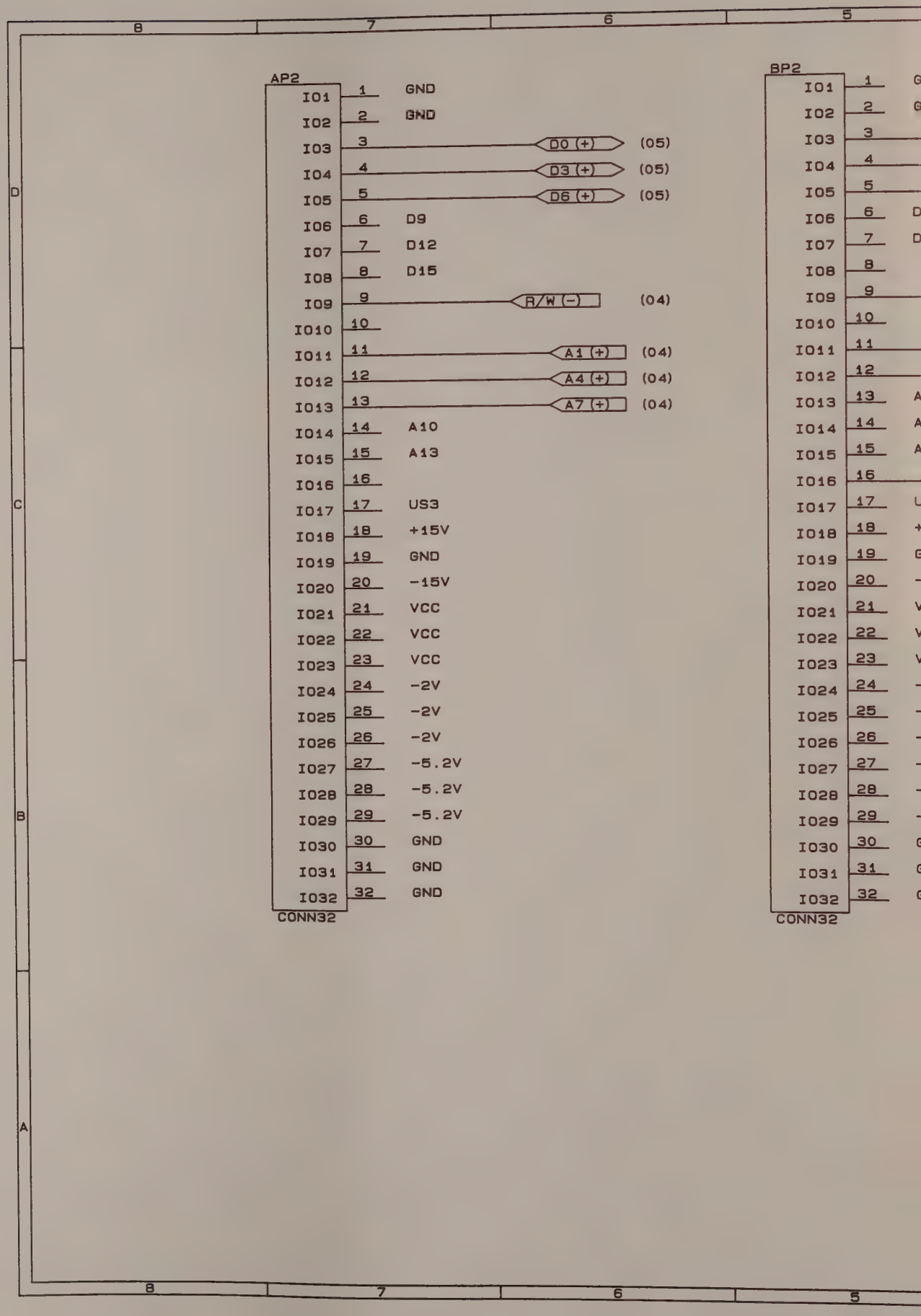
SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	20747	LD500-0989	—

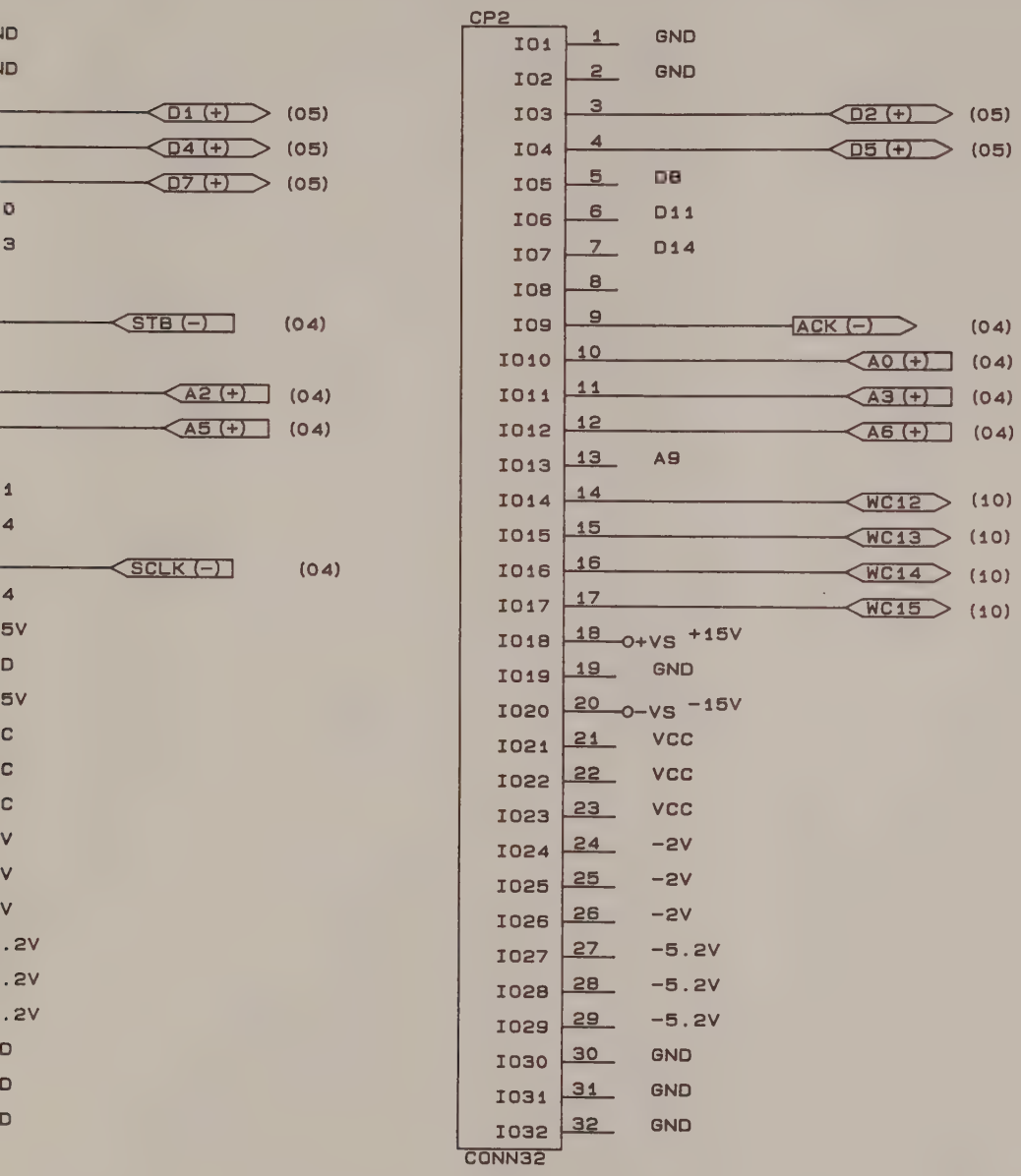
SHEET NO. 00 OF 22


AP1
IO1 1
IO2 2
IO3 3
IO4 4
IO5 5
IO6 6
IO7 7
IO8 8
IO9 9
IO10 10
IO11 11
IO12 12
IO13 13
IO14 14
IO15 15
IO16 16
IO17 17
IO18 18
IO19 19
IO20 20
IO21 21
IO22 22
IO23 23
IO24 24
IO25 25
IO26 26
IO27 27
IO28 28
IO29 29
IO30 30
IO31 31
IO32 32
CONN32
DAC 1 (13)
DAC 2 (13)
DAC 3 (14)
DAC 4 (14)
DAC 5 (15)
DAC 6 (15)
DAC 7 (16)
DAC 8 (16)
DAC 9 (17)
DAC 10 (17)
DAC 11 (18)
DAC 12 (18)
DAC 13 (19)
DAC 14 (19)
DAC 15 (20)
DAC 16 (20)
BP1
IO1 1
IO2 2
IO3 3
IO4 4
IO5 5
IO6 6
IO7 7
IO8 8
IO9 9
IO10 10
IO11 11
IO12 12
IO13 13
IO14 14
IO15 15
IO16 16
IO17 17
IO18 18
IO19 19
IO20 20
IO21 21
IO22 22
IO23 23
IO24 24
IO25 25
IO26 26
IO27 27
IO28 28
IO29 29
IO30 30
IO31 31
IO32 32
CONN32

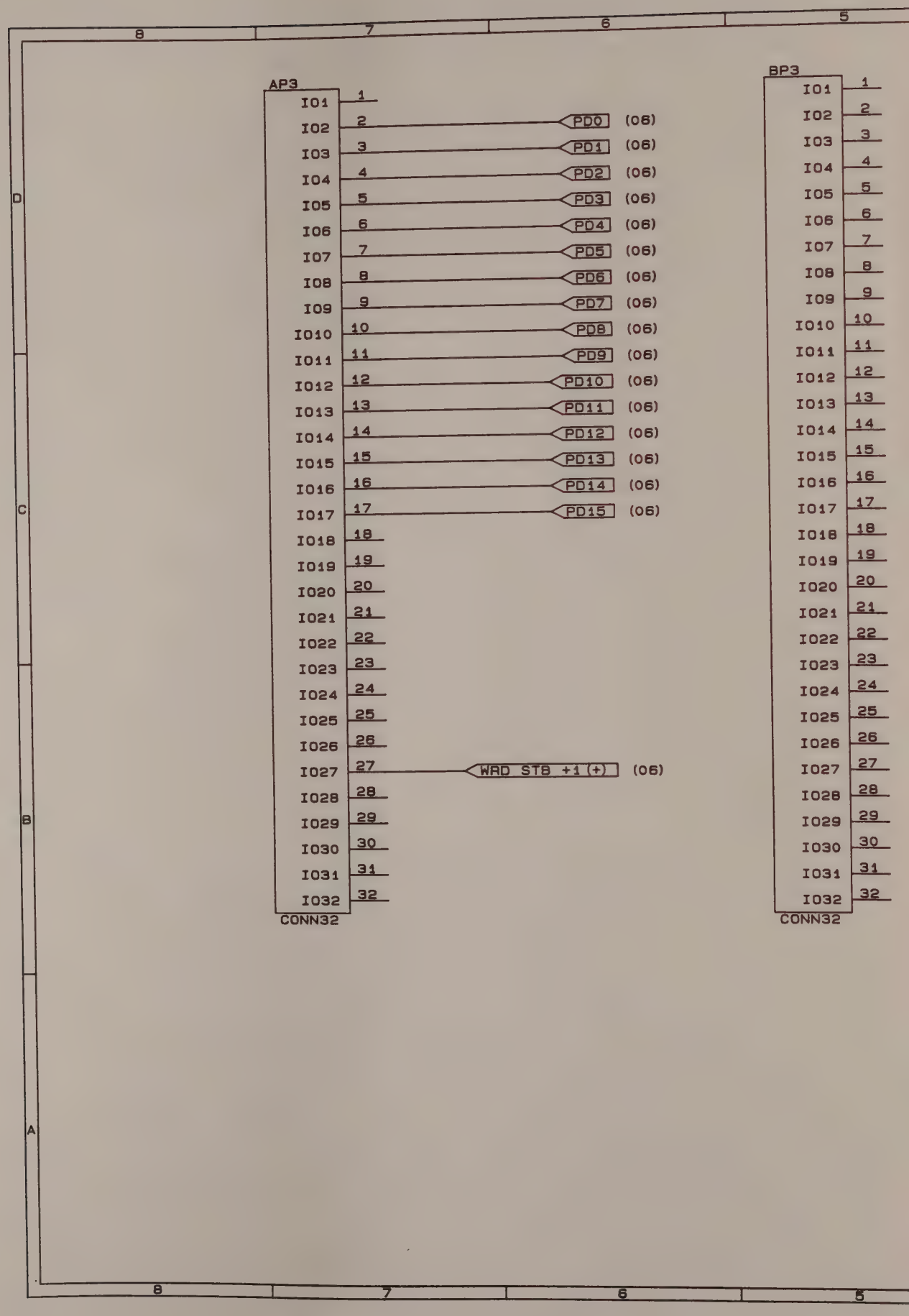


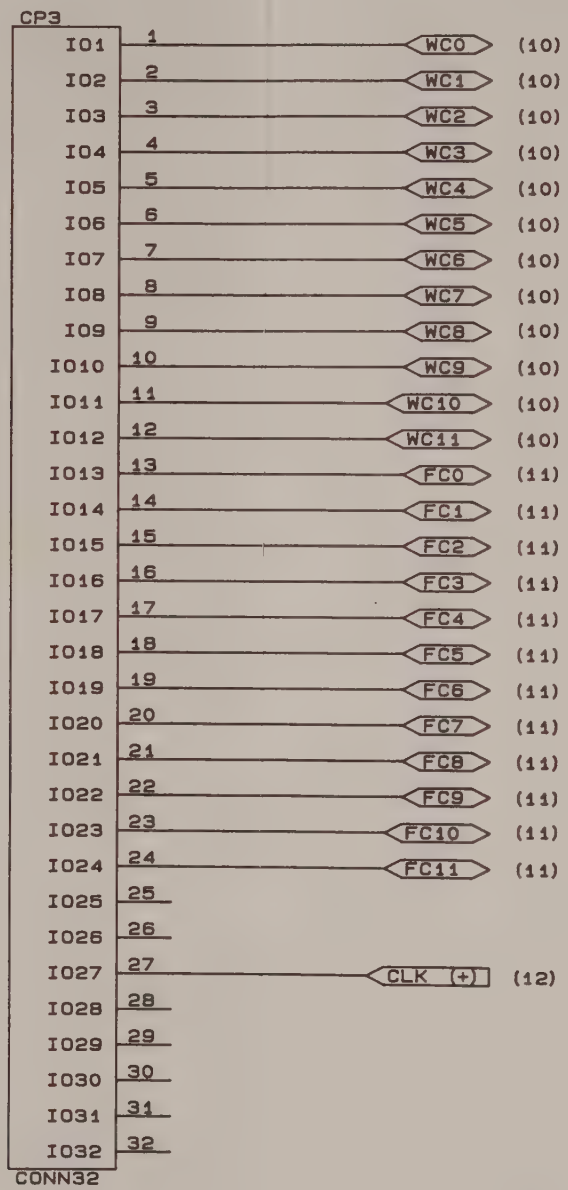
P1 CONNECTOR DAC & DER OUTPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 1 OF 22			


8
7
6
5
D
C
B
A
AP2
IO1 1 GND
IO2 2 GND
IO3 3 D0 (+) (05)
IO4 4 D3 (+) (05)
IO5 5 D6 (+) (05)
IO6 6 D9
IO7 7 D12
IO8 8 D15
IO9 9 R/W (-) (04)
IO10 10
IO11 11 A1 (+) (04)
IO12 12 A4 (+) (04)
IO13 13 A7 (+) (04)
IO14 14 A10
IO15 15 A13
IO16 16
IO17 17 US3
IO18 18 +15V
IO19 19 GND
IO20 20 -15V
IO21 21 VCC
IO22 22 VCC
IO23 23 VCC
IO24 24 -2V
IO25 25 -2V
IO26 26 -2V
IO27 27 -5.2V
IO28 28 -5.2V
IO29 29 -5.2V
IO30 30 GND
IO31 31 GND
IO32 32 GND
CONN32
BP2
IO1 1
IO2 2
IO3 3
IO4 4
IO5 5
IO6 6
IO7 7
IO8 8
IO9 9
IO10 10
IO11 11
IO12 12
IO13 13
IO14 14
IO15 15
IO16 16
IO17 17
IO18 18
IO19 19
IO20 20
IO21 21
IO22 22
IO23 23
IO24 24
IO25 25
IO26 26
IO27 27
IO28 28
IO29 29
IO30 30
IO31 31
IO32 32
CONN32

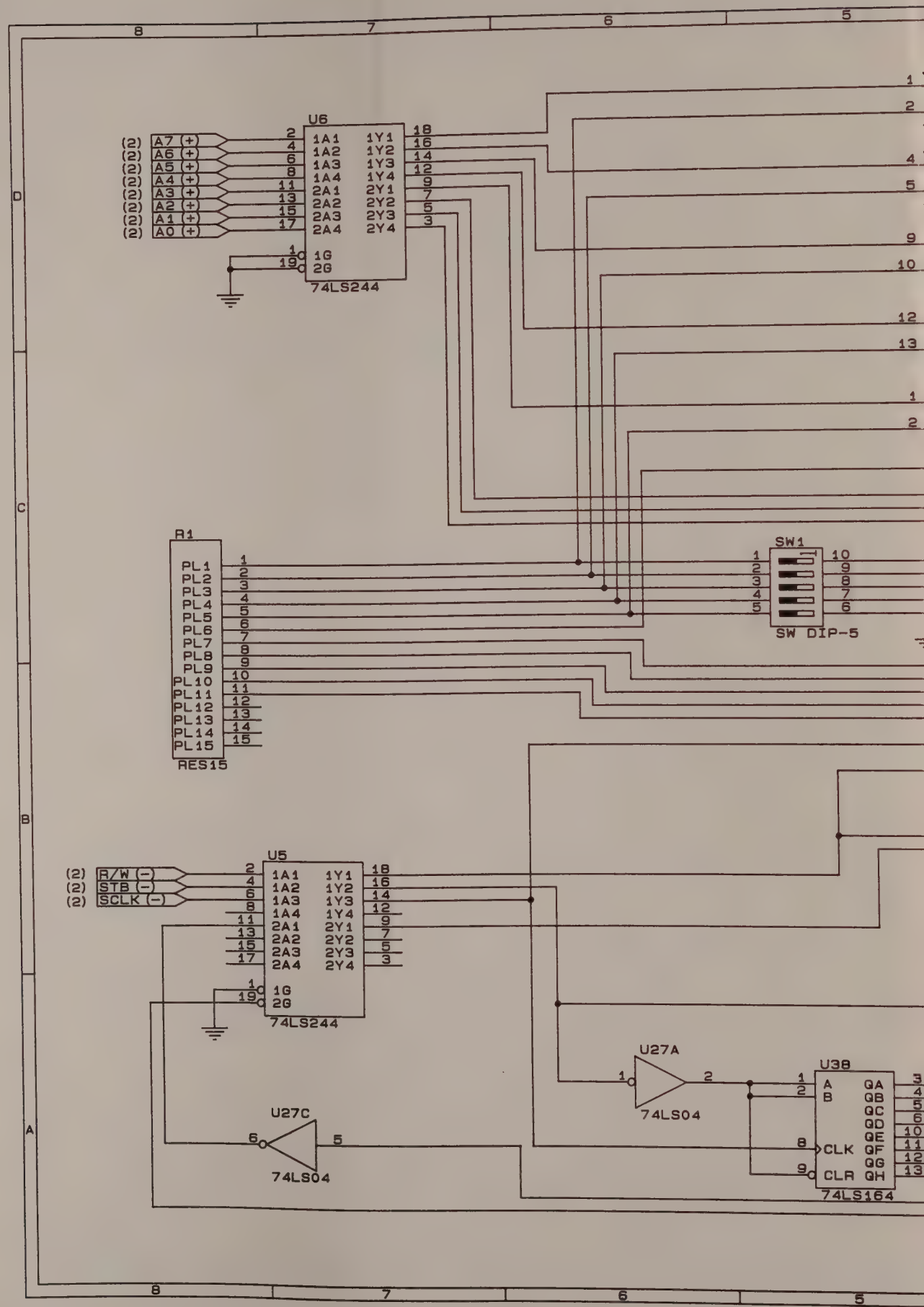


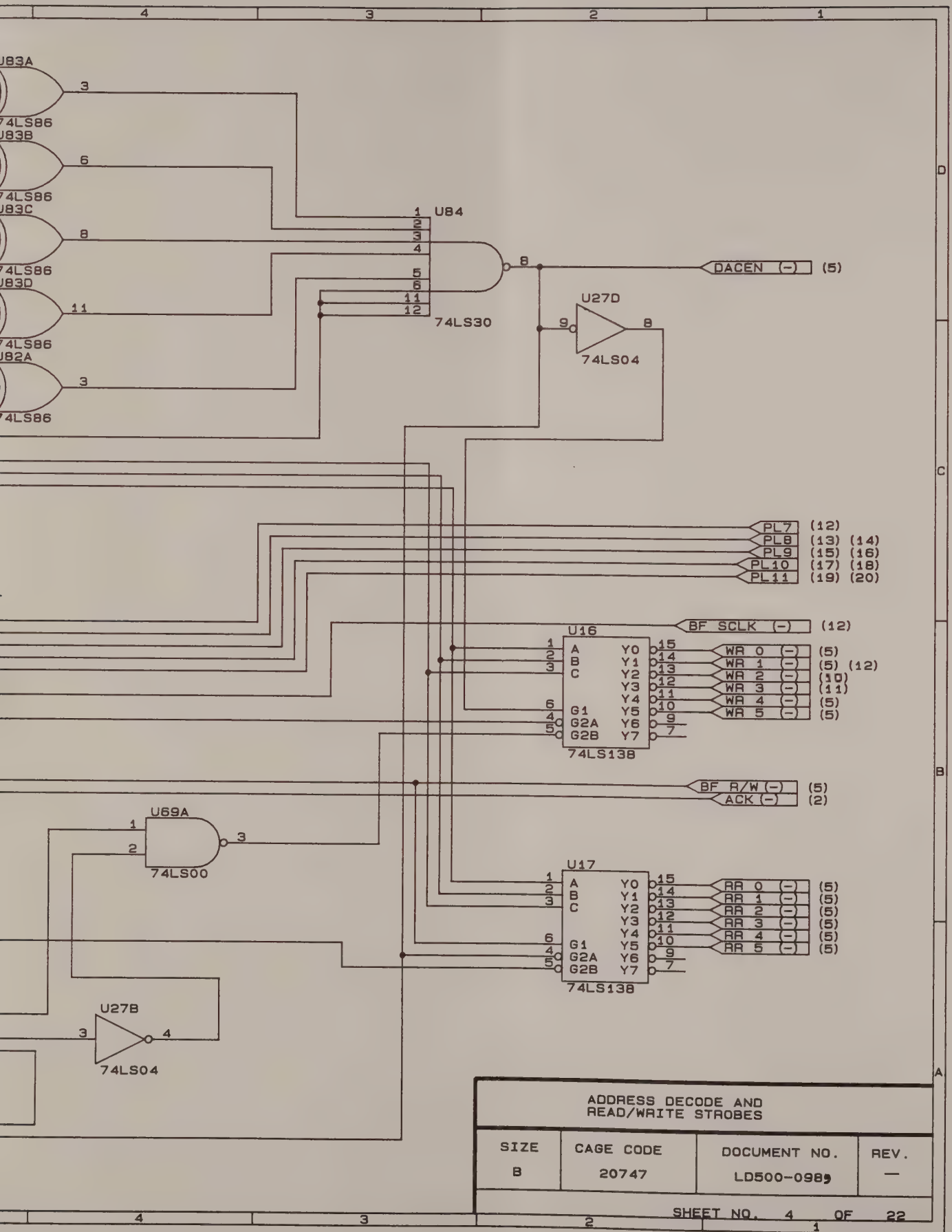
P2 CONNECTOR IOC BUS POWER			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 2 OF 22			


8
7
6
5
D
C
B
A
AP3
IO1 1
IO2 2
IO3 3
IO4 4
IO5 5
IO6 6
IO7 7
IO8 8
IO9 9
IO10 10
IO11 11
IO12 12
IO13 13
IO14 14
IO15 15
IO16 16
IO17 17
IO18 18
IO19 19
IO20 20
IO21 21
IO22 22
IO23 23
IO24 24
IO25 25
IO26 26
IO27 27
IO28 28
IO29 29
IO30 30
IO31 31
IO32 32
CONN32
PD0 (06)
PD1 (06)
PD2 (06)
PD3 (06)
PD4 (06)
PD5 (06)
PD6 (06)
PD7 (06)
PD8 (06)
PD9 (06)
PD10 (06)
PD11 (06)
PD12 (06)
PD13 (06)
PD14 (06)
PD15 (06)
WRD STB +1 (+) (06)
BP3
IO1 1
IO2 2
IO3 3
IO4 4
IO5 5
IO6 6
IO7 7
IO8 8
IO9 9
IO10 10
IO11 11
IO12 12
IO13 13
IO14 14
IO15 15
IO16 16
IO17 17
IO18 18
IO19 19
IO20 20
IO21 21
IO22 22
IO23 23
IO24 24
IO25 25
IO26 26
IO27 27
IO28 28
IO29 29
IO30 30
IO31 31
IO32 32
CONN32

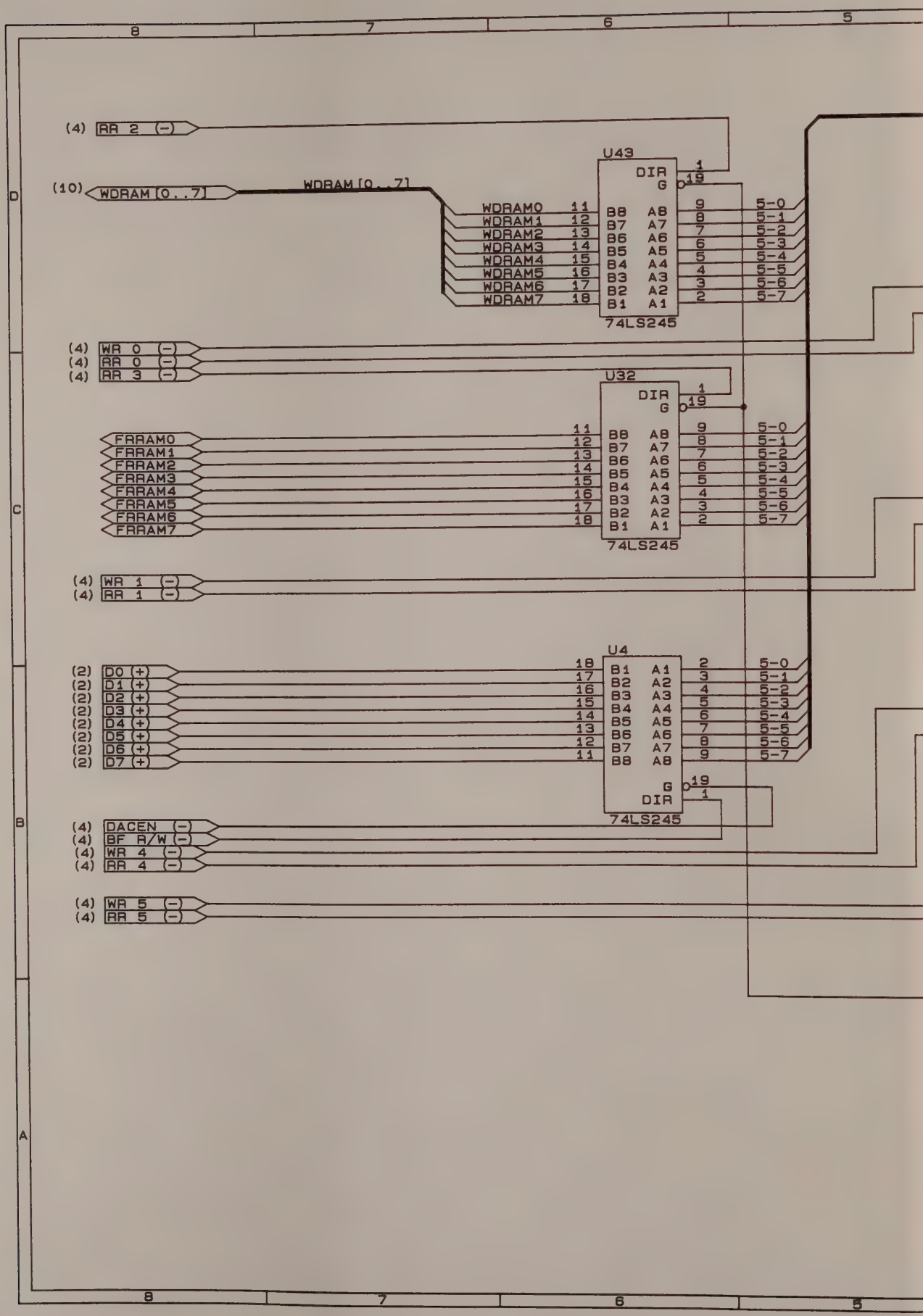


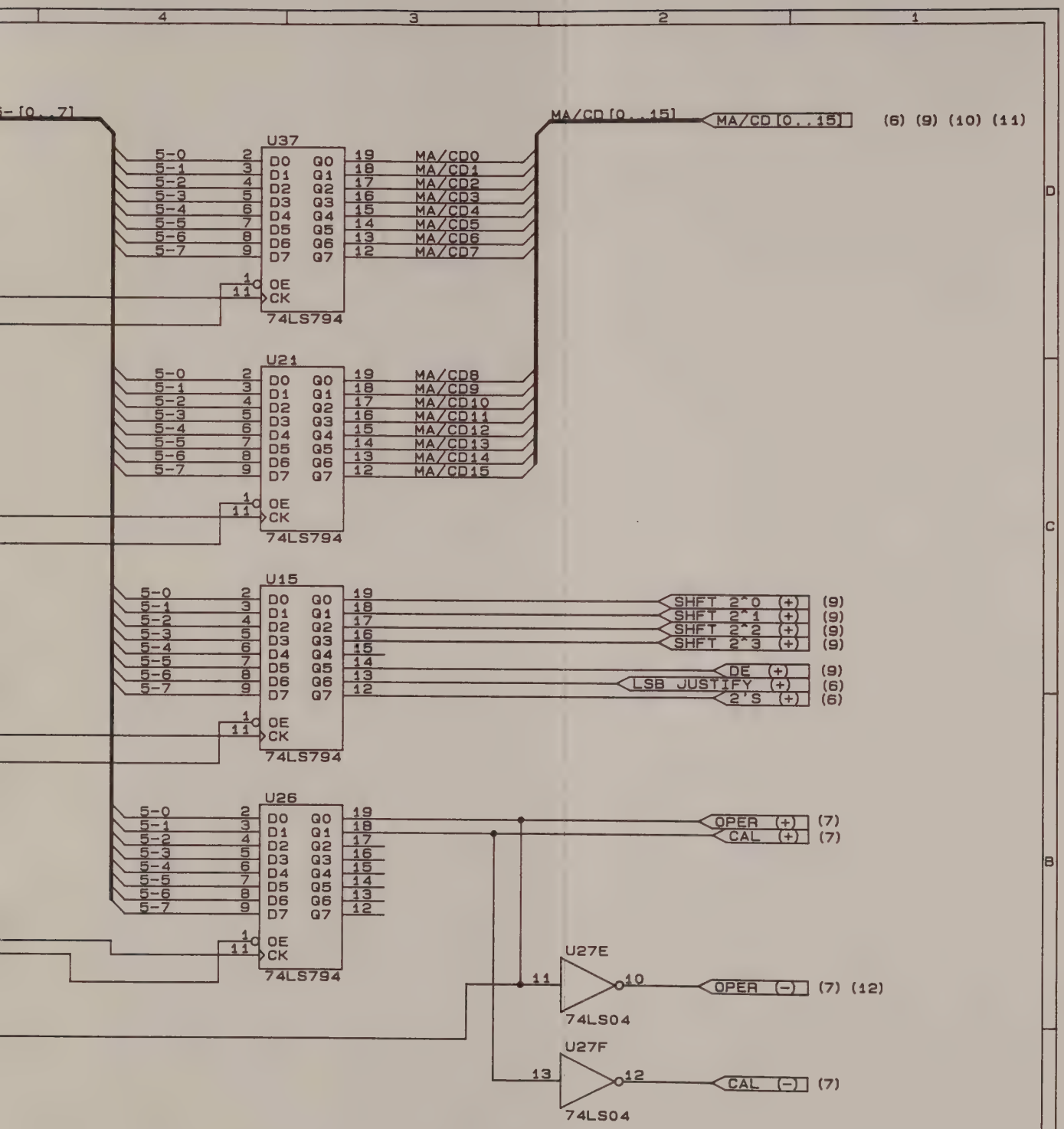
P3 CONNECTOR FRAME SYNC INPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 3 OF 22			


U6
(2) A7 (+)
(2) A6 (+)
(2) A5 (+)
(2) A4 (+)
(2) A3 (+)
(2) A2 (+)
(2) A1 (+)
(2) A0 (+)
1A1 1A2 1A3 1A4 2A1 2A2 2A3 2A4
1Y1 1Y2 1Y3 1Y4 2Y1 2Y2 2Y3 2Y4
1G 2G
74LS244
R1
PL1 PL2 PL3 PL4 PL5 PL6 PL7 PL8 PL9 PL10 PL11 PL12 PL13 PL14 PL15
RES15
SW1
SW DIP-5
U5
(2) R/W (-)
(2) STB (-)
(2) SCLK (-)
74LS244
U27A
74LS04
U27C
74LS04
U38
A B CLK CLR
QA QB QC QD QE QF QG QH
74LS164

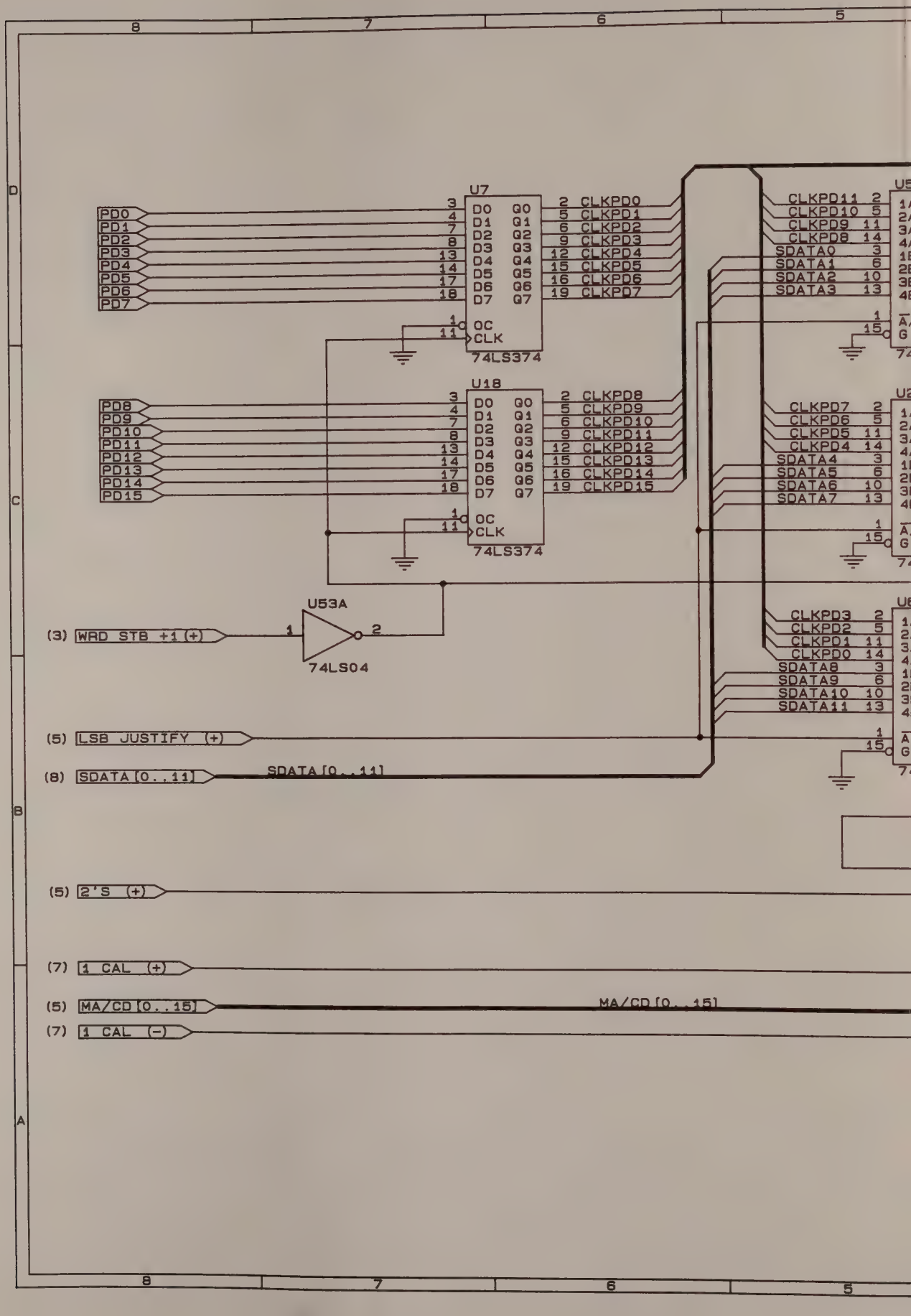


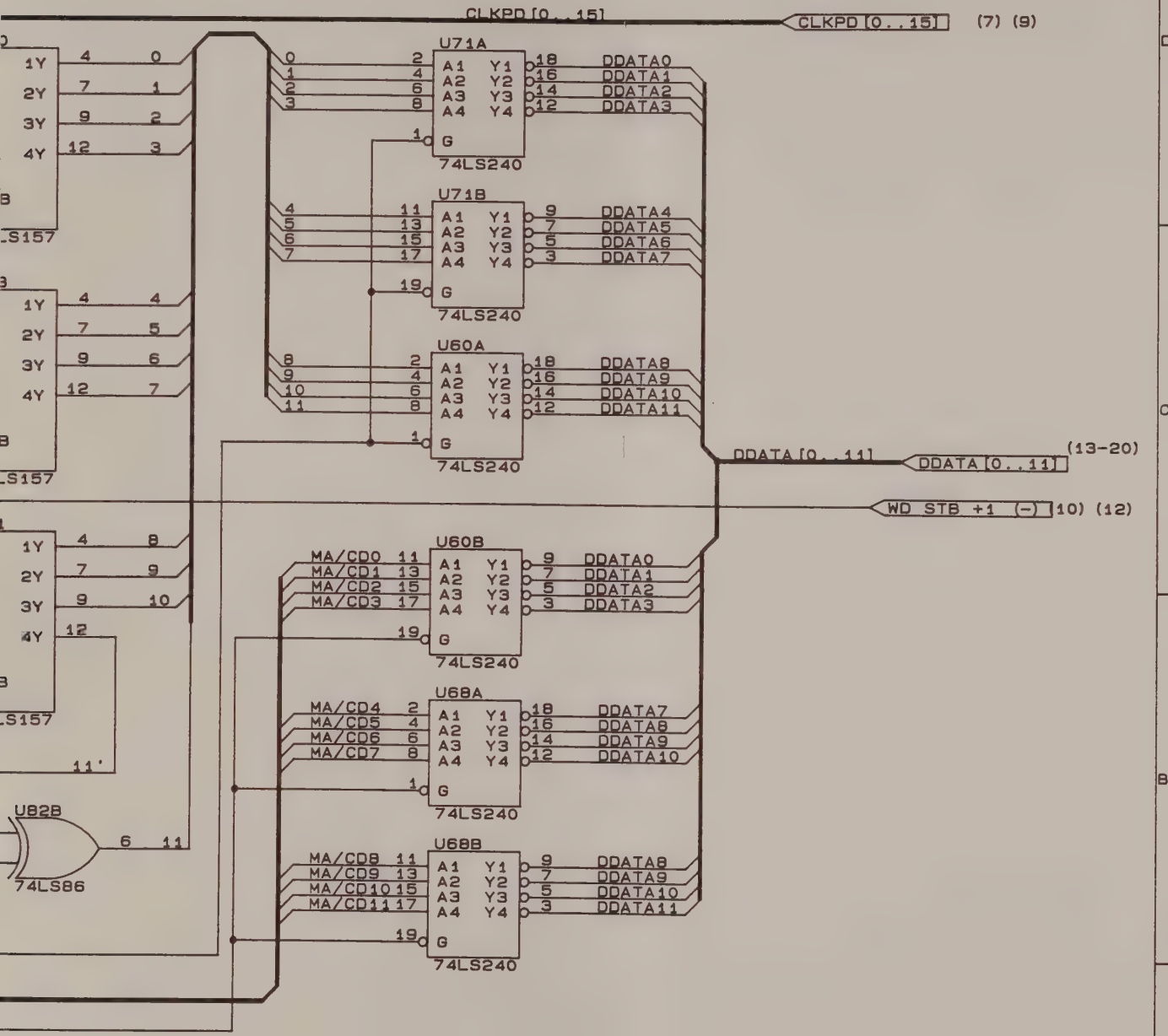
ADDRESS DECODE AND READ/WRITE STROBES			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 4 OF 22			


8
7
6
5
D
C
B
A
(4) RA 2 (-)
U43
DIR
G
1
19
(10) WDRAM[0..7]
WDRAM[0..7]
WDRAM0 11
WDRAM1 12
WDRAM2 13
WDRAM3 14
WDRAM4 15
WDRAM5 16
WDRAM6 17
WDRAM7 18
B8 A8 9 5-0
B7 A7 8 5-1
B6 A6 7 5-2
B5 A5 6 5-3
B4 A4 5 5-4
B3 A3 4 5-5
B2 A2 3 5-6
B1 A1 2 5-7
74LS245
(4) WR 0 (-)
(4) RA 0 (-)
(4) RA 3 (-)
U32
DIR
G
1
19
FRRAM0 11
FRRAM1 12
FRRAM2 13
FRRAM3 14
FRRAM4 15
FRRAM5 16
FRRAM6 17
FRRAM7 18
B8 A8 9 5-0
B7 A7 8 5-1
B6 A6 7 5-2
B5 A5 6 5-3
B4 A4 5 5-4
B3 A3 4 5-5
B2 A2 3 5-6
B1 A1 2 5-7
74LS245
(4) WR 1 (-)
(4) RA 1 (-)
U4
(2) D0 (+) 18
(2) D1 (+) 17
(2) D2 (+) 16
(2) D3 (+) 15
(2) D4 (+) 14
(2) D5 (+) 13
(2) D6 (+) 12
(2) D7 (+) 11
B1 A1 2 5-0
B2 A2 3 5-1
B3 A3 4 5-2
B4 A4 5 5-3
B5 A5 6 5-4
B6 A6 7 5-5
B7 A7 8 5-6
B8 A8 9 5-7
G 19
DIR 1
74LS245
(4) DACEN (-)
(4) BF R/W (-)
(4) WR 4 (-)
(4) RA 4 (-)
(4) WR 5 (-)
(4) RA 5 (-)
8
7
6
5

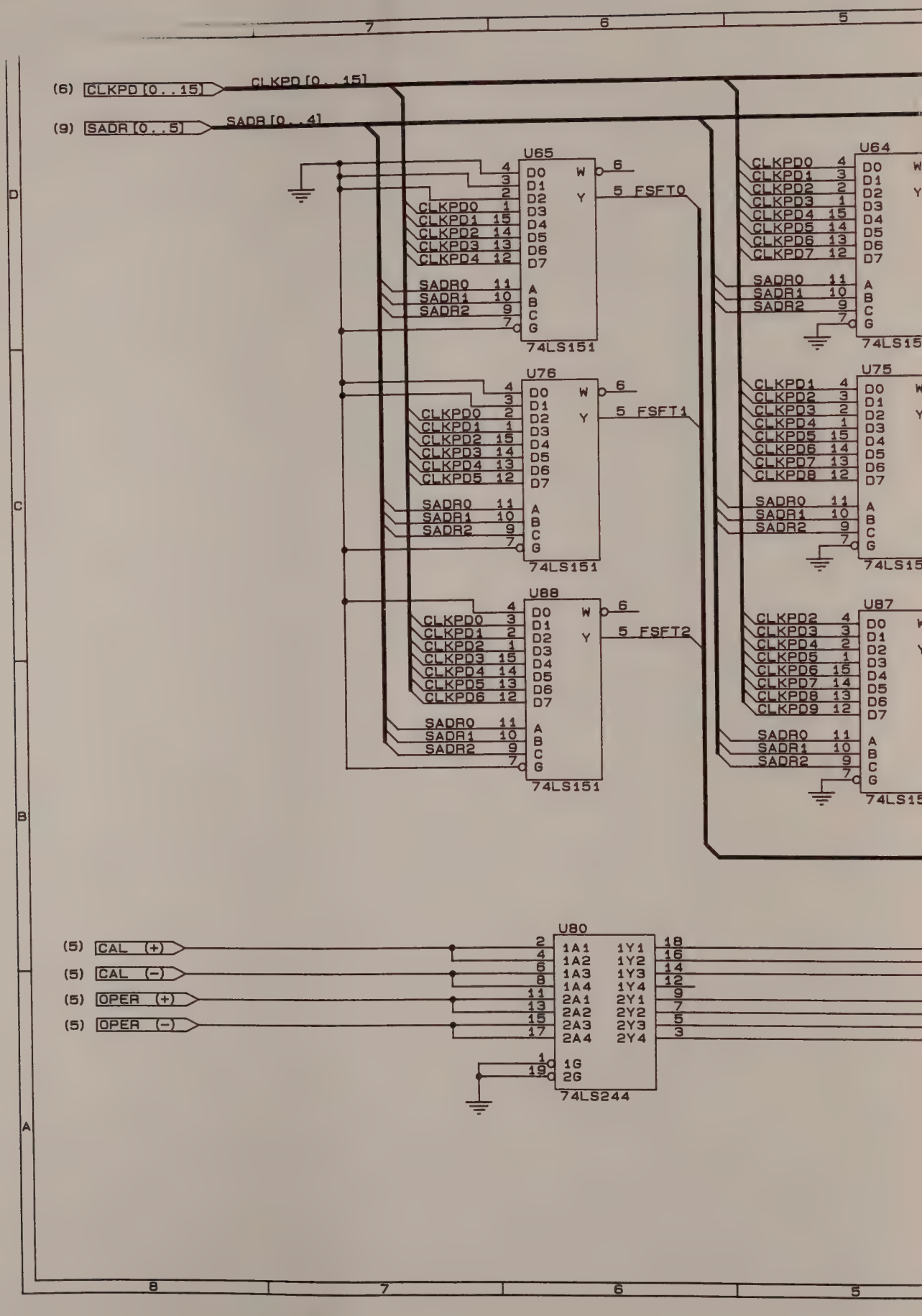


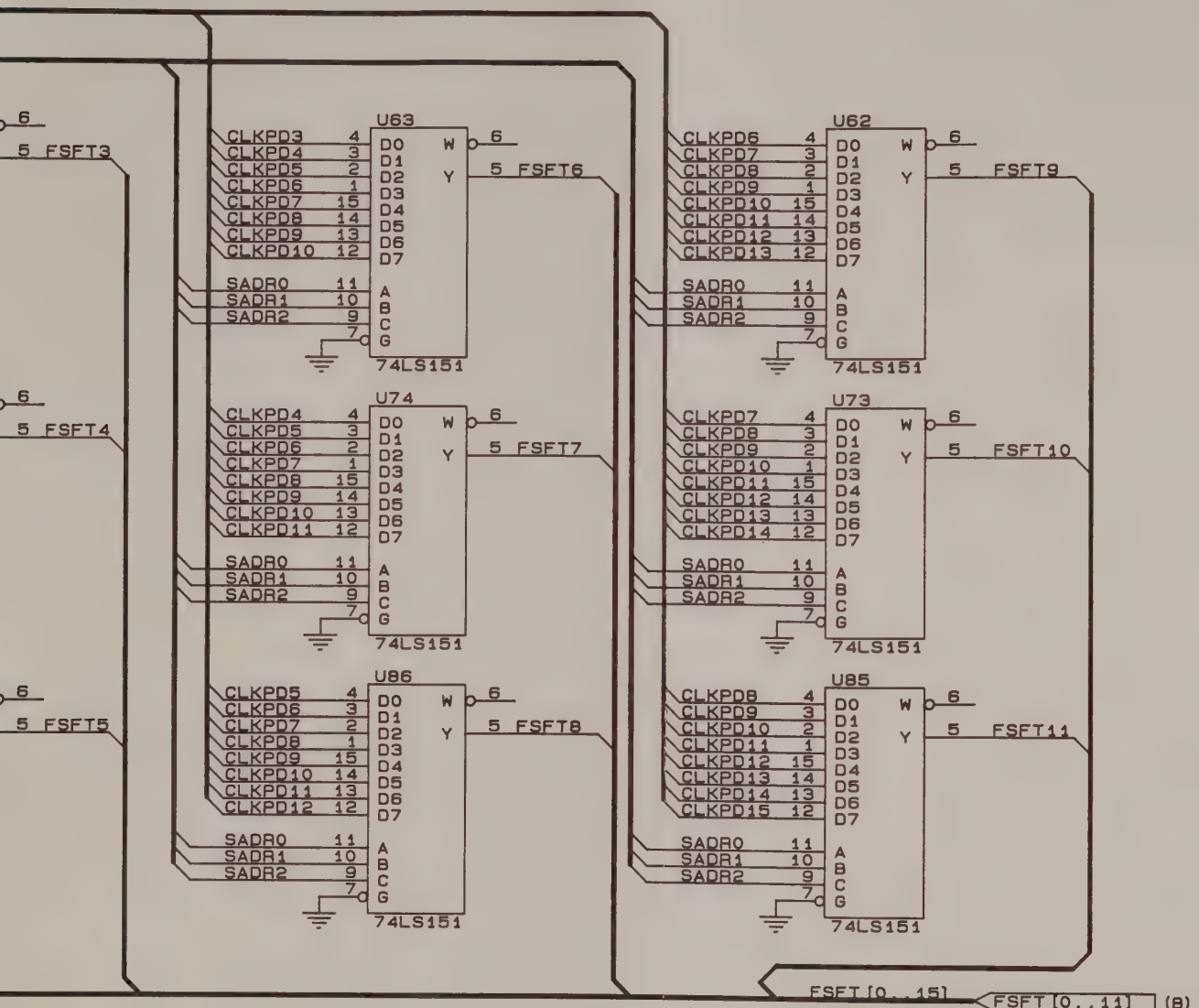
DAC SETUP REGISTERS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 5 OF 22			

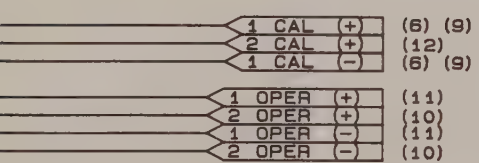

8
7
6
5
D
C
B
A
U7
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
D0 Q0
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
D7 Q7
OC
CLK
74LS374
CLKPD0
CLKPD1
CLKPD2
CLKPD3
CLKPD4
CLKPD5
CLKPD6
CLKPD7
U18
PD8
PD9
PD10
PD11
PD12
PD13
PD14
PD15
CLKPD8
CLKPD9
CLKPD10
CLKPD11
CLKPD12
CLKPD13
CLKPD14
CLKPD15
U53A
74LS04
(3) WRD STB +1 (+)
(5) LSB JUSTIFY (+)
(8) SDATA [0..11]
SDATA [0..11]
(5) 2'S (+)
(7) 1 CAL (+)
(5) MA/CD [0..15]
MA/CD [0..15]
(7) 1 CAL (-)
CLKPD11
CLKPD10
CLKPD9
CLKPD8
SDATA0
SDATA1
SDATA2
SDATA3
SDATA4
SDATA5
SDATA6
SDATA7
SDATA8
SDATA9
SDATA10
SDATA11



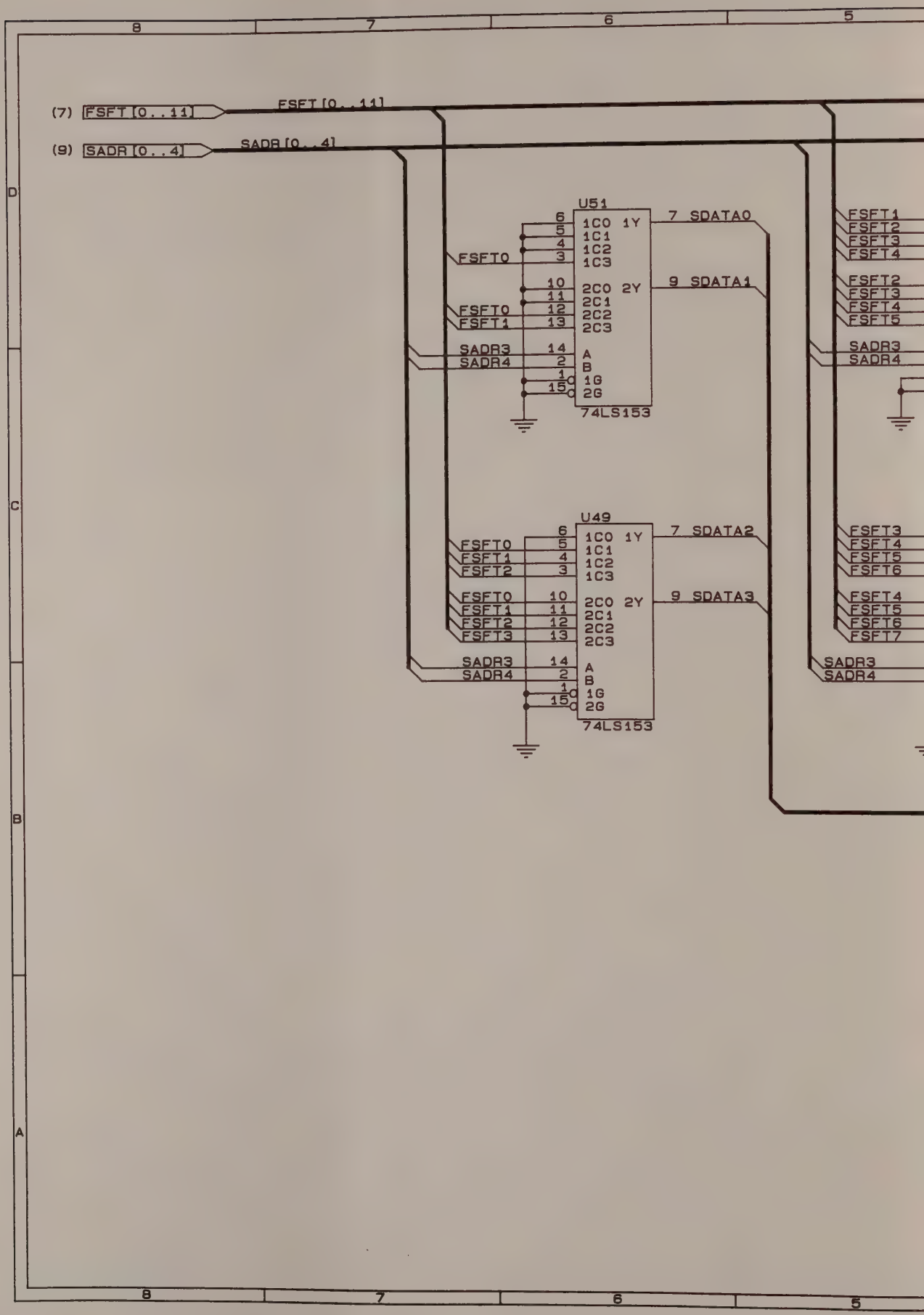
DAC DATA GENERATION			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 6 OF			

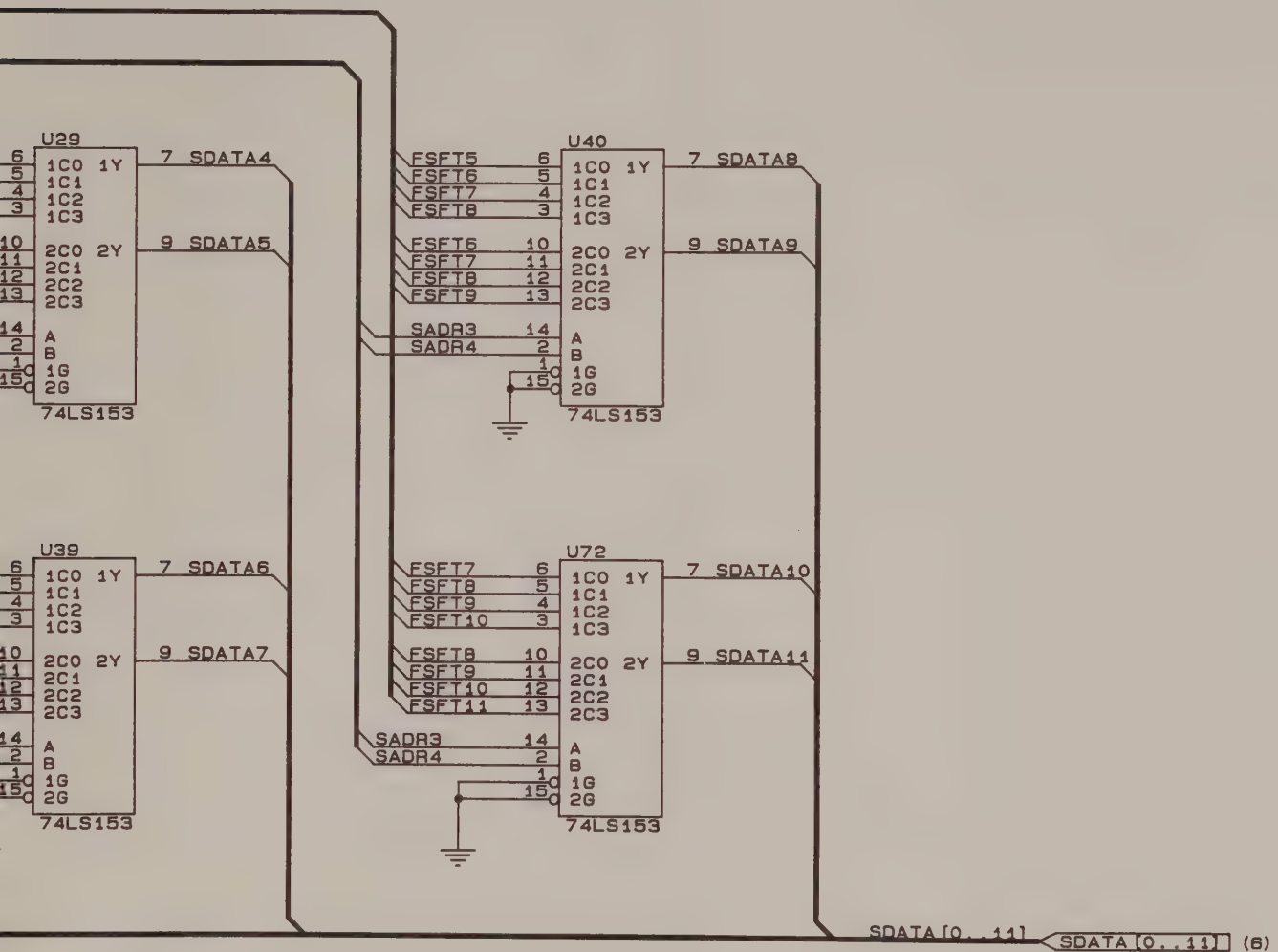

(6) CLKPD [0..15]
CLKPD [0..15]
(9) SADR [0..5]
SADR [0..4]
U65
74LS151
5 FSFT0
U76
74LS151
5 FSFT1
U88
74LS151
5 FSFT2
U64
74LS15
U75
74LS15
U87
74LS15
(5) CAL (+)
(5) CAL (-)
(5) OPER (+)
(5) OPER (-)
U80
74LS244



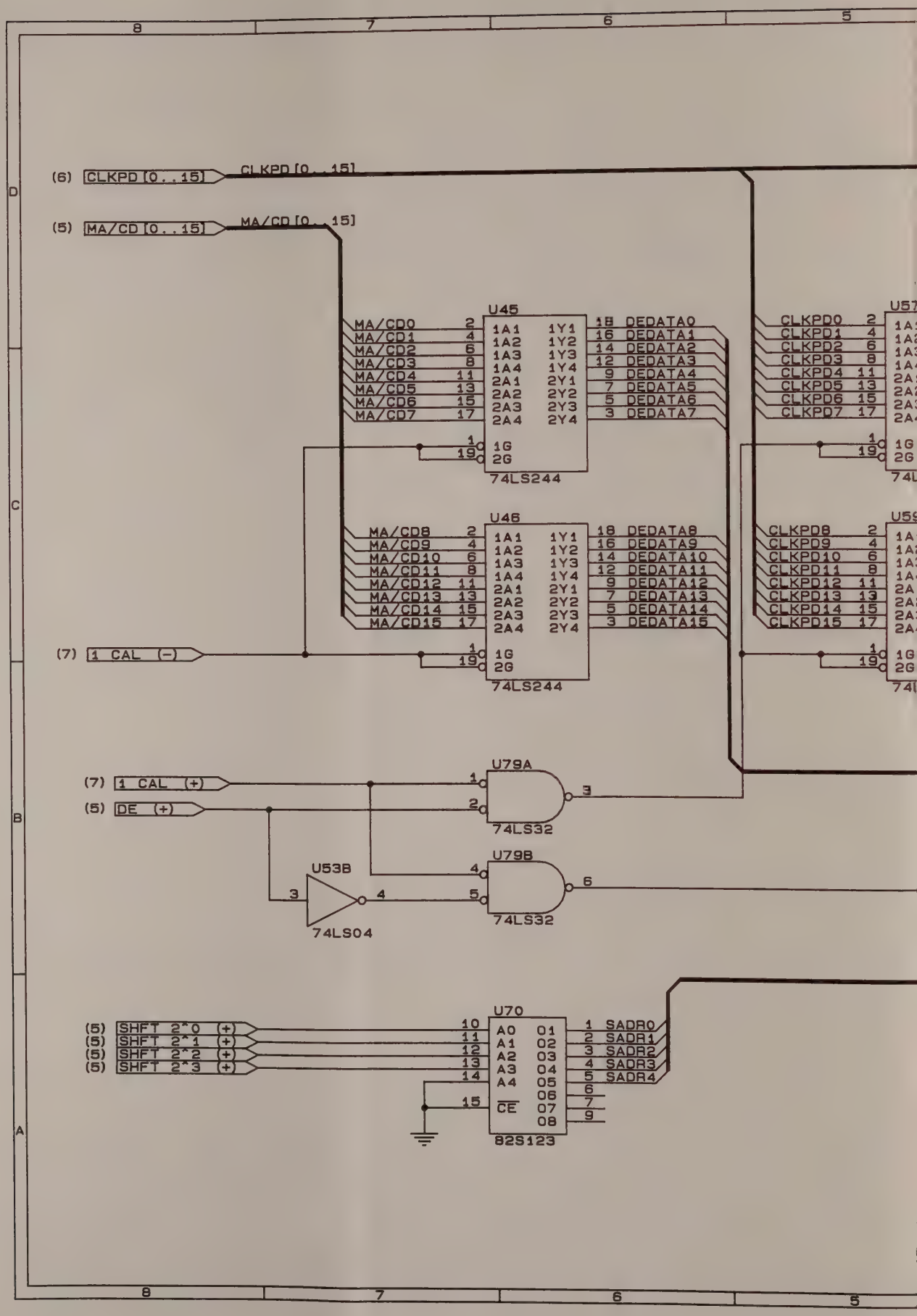


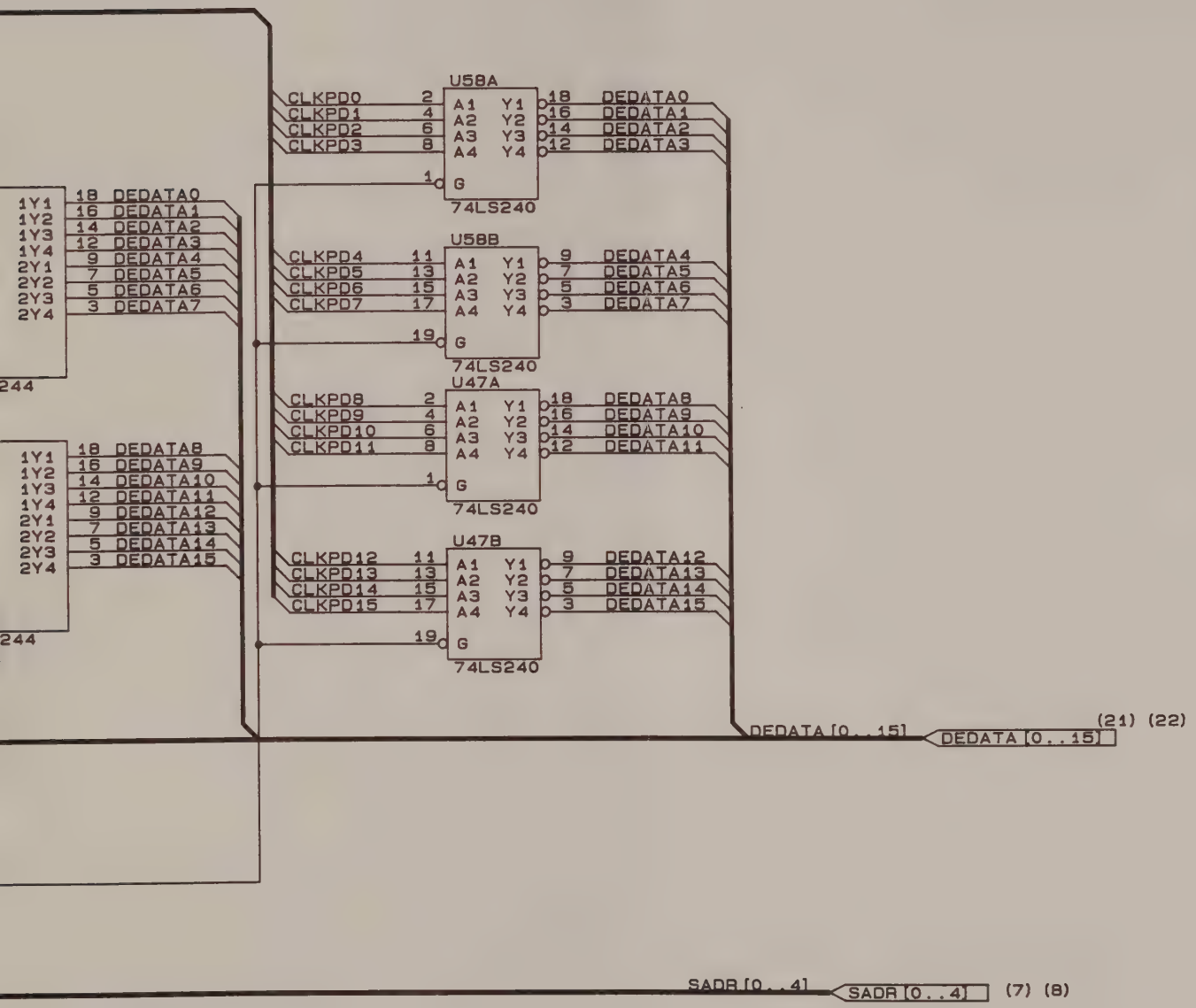
FIRST STAGE OF DAC DATA SHIFT			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 7 OF 22			


8
7
6
5
D
C
B
A
(7) FSFT[0..11]
FSFT[0..11]
(9) SADR[0..4]
SADR[0..4]
U51
1C0 1Y
1C1
1C2
1C3
2C0 2Y
2C1
2C2
2C3
A
B
1G
2G
74LS153
FSFT0
FSFT1
SADR3
SADR4
7 SDATA0
9 SDATA1
U49
7 SDATA2
9 SDATA3
FSFT2
FSFT3
FSFT4
FSFT5
FSFT6
FSFT7

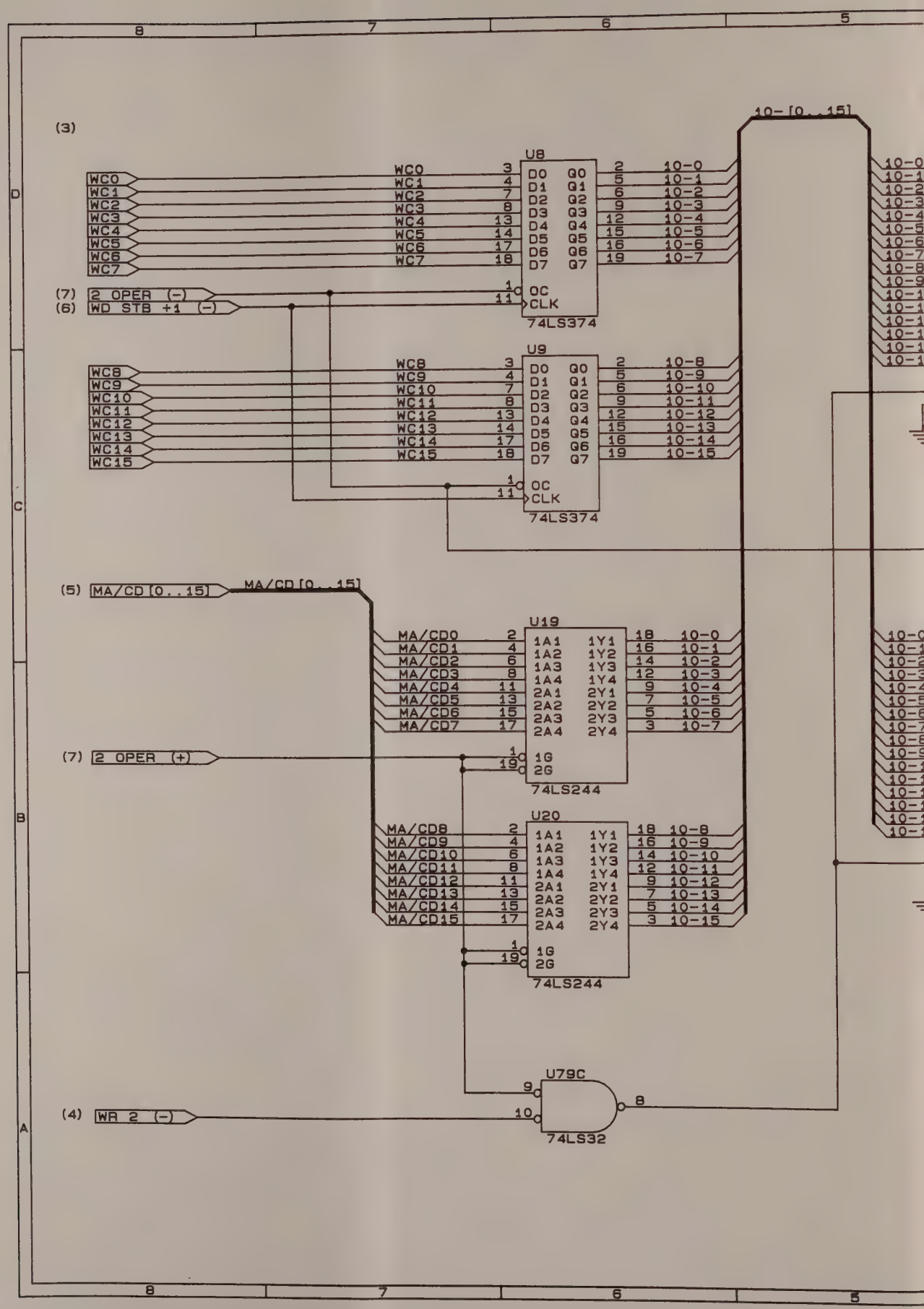


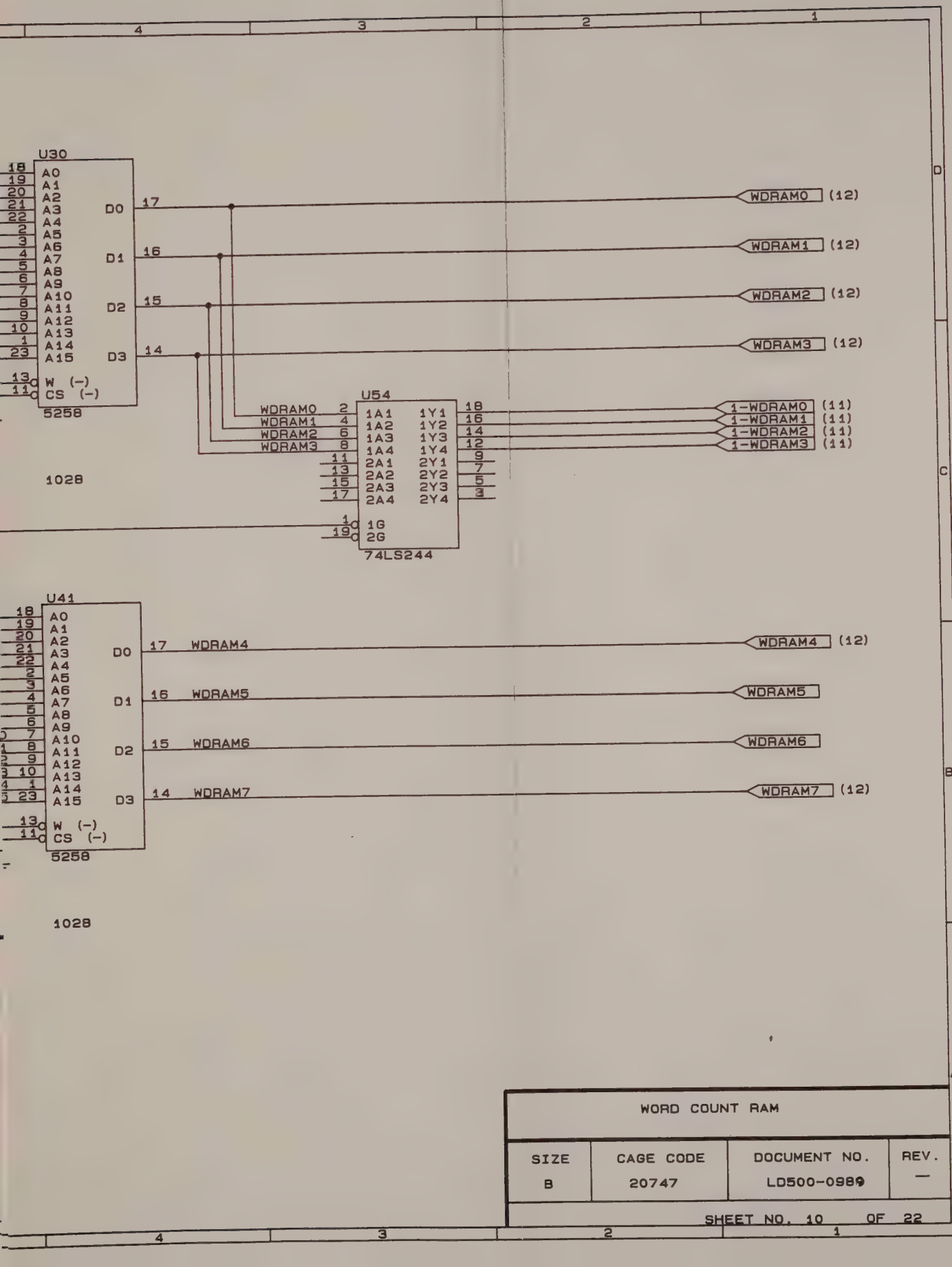
SECOND STAGE OF DAC DATA SHIFT			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
		SHEET NO. 8 OF 22	


8
7
6
5
D
C
B
A
(6) CLKPD[0..15]
CLKPD[0..15]
(5) MA/CD[0..15]
MA/CD[0..15]
U45
MA/CD0 2
MA/CD1 4
MA/CD2 6
MA/CD3 8
MA/CD4 11
MA/CD5 13
MA/CD6 15
MA/CD7 17
1A1 1Y1 18 DEDATA0
1A2 1Y2 16 DEDATA1
1A3 1Y3 14 DEDATA2
1A4 1Y4 12 DEDATA3
2A1 2Y1 9 DEDATA4
2A2 2Y2 7 DEDATA5
2A3 2Y3 5 DEDATA6
2A4 2Y4 3 DEDATA7
1 1G
19 2G
74LS244
U46
MA/CD8 2
MA/CD9 4
MA/CD10 6
MA/CD11 8
MA/CD12 11
MA/CD13 13
MA/CD14 15
MA/CD15 17
1A1 1Y1 18 DEDATA8
1A2 1Y2 16 DEDATA9
1A3 1Y3 14 DEDATA10
1A4 1Y4 12 DEDATA11
2A1 2Y1 9 DEDATA12
2A2 2Y2 7 DEDATA13
2A3 2Y3 5 DEDATA14
2A4 2Y4 3 DEDATA15
1 1G
19 2G
74LS244
(7) 1 CAL (-)
U79A
(7) 1 CAL (+)
(5) DE (+)
1
2
3
74LS32
U53B
3
4
74LS04
U79B
4
5
6
74LS32
U70
(5) SHFT 2^0 (+)
(5) SHFT 2^1 (+)
(5) SHFT 2^2 (+)
(5) SHFT 2^3 (+)
10 A0 01 1 SADR0
11 A1 02 2 SADR1
12 A2 03 3 SADR2
13 A3 04 4 SADR3
14 A4 05 5 SADR4
06 6
15 CE 07 7
08 9
82S123

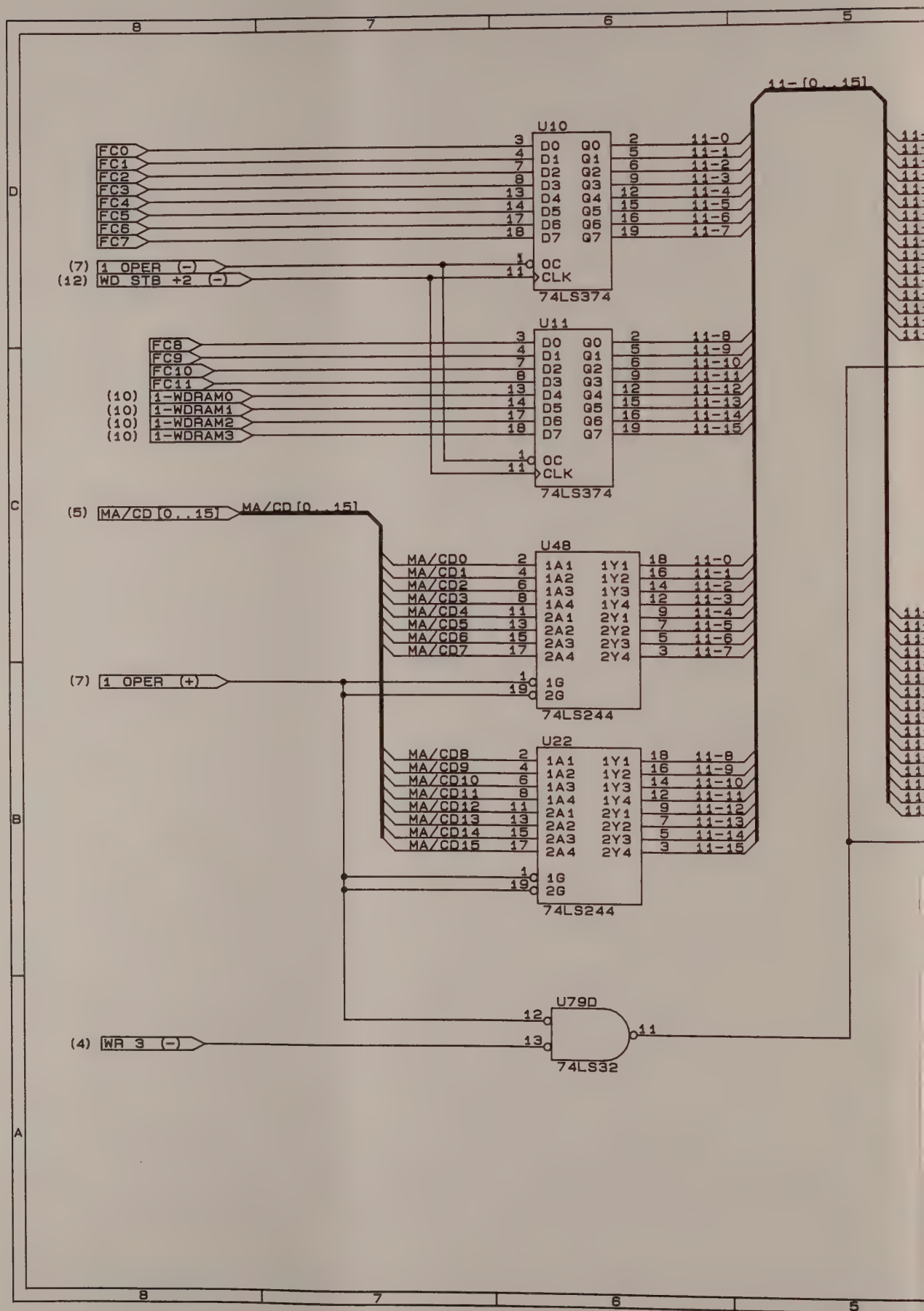


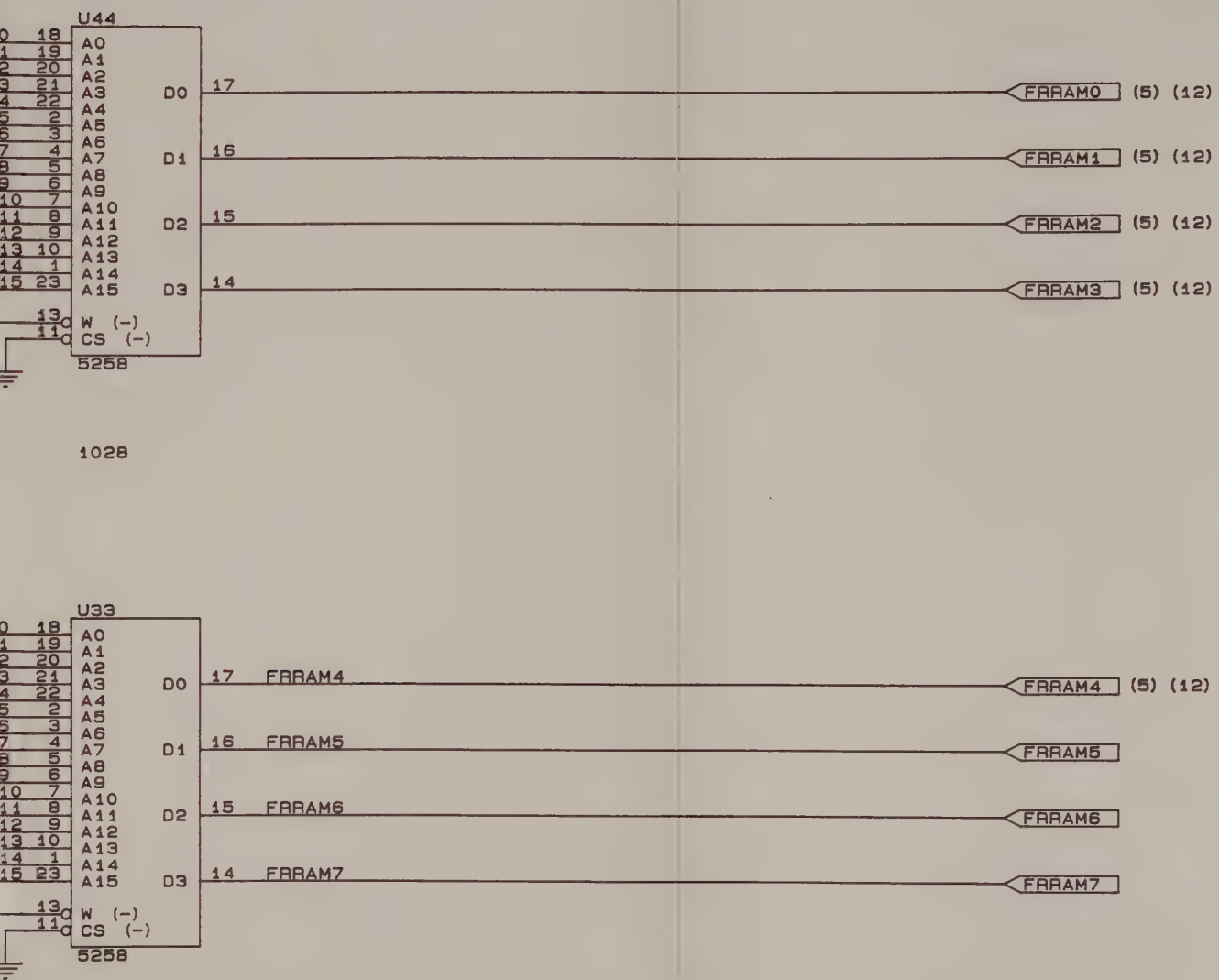
DIGITAL EVENT DATA GENERATION AND SHIFT ADDRESS GENERATION			
SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	20747	LD500-0989	—
		SHEET NO. 9 OF 22	


8
7
6
5
D
C
B
A
(3)
10-[0..15]
U8
WC0
WC1
WC2
WC3
WC4
WC5
WC6
WC7
D0 Q0
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
D7 Q7
10-0
10-1
10-2
10-3
10-4
10-5
10-6
10-7
(7) 2 OPER (-)
(6) WD STB +1 (-)
OC
CLK
74LS374
U9
WC8
WC9
WC10
WC11
WC12
WC13
WC14
WC15
10-8
10-9
10-10
10-11
10-12
10-13
10-14
10-15
74LS374
(5) MA/CD[0..15]
MA/CD[0..15]
U19
MA/CD0
MA/CD1
MA/CD2
MA/CD3
MA/CD4
MA/CD5
MA/CD6
MA/CD7
1A1 1Y1
1A2 1Y2
1A3 1Y3
1A4 1Y4
2A1 2Y1
2A2 2Y2
2A3 2Y3
2A4 2Y4
(7) 2 OPER (+)
1G
2G
74LS244
U20
MA/CD8
MA/CD9
MA/CD10
MA/CD11
MA/CD12
MA/CD13
MA/CD14
MA/CD15
74LS244
U79C
(4) WR 2 (-)
74LS32

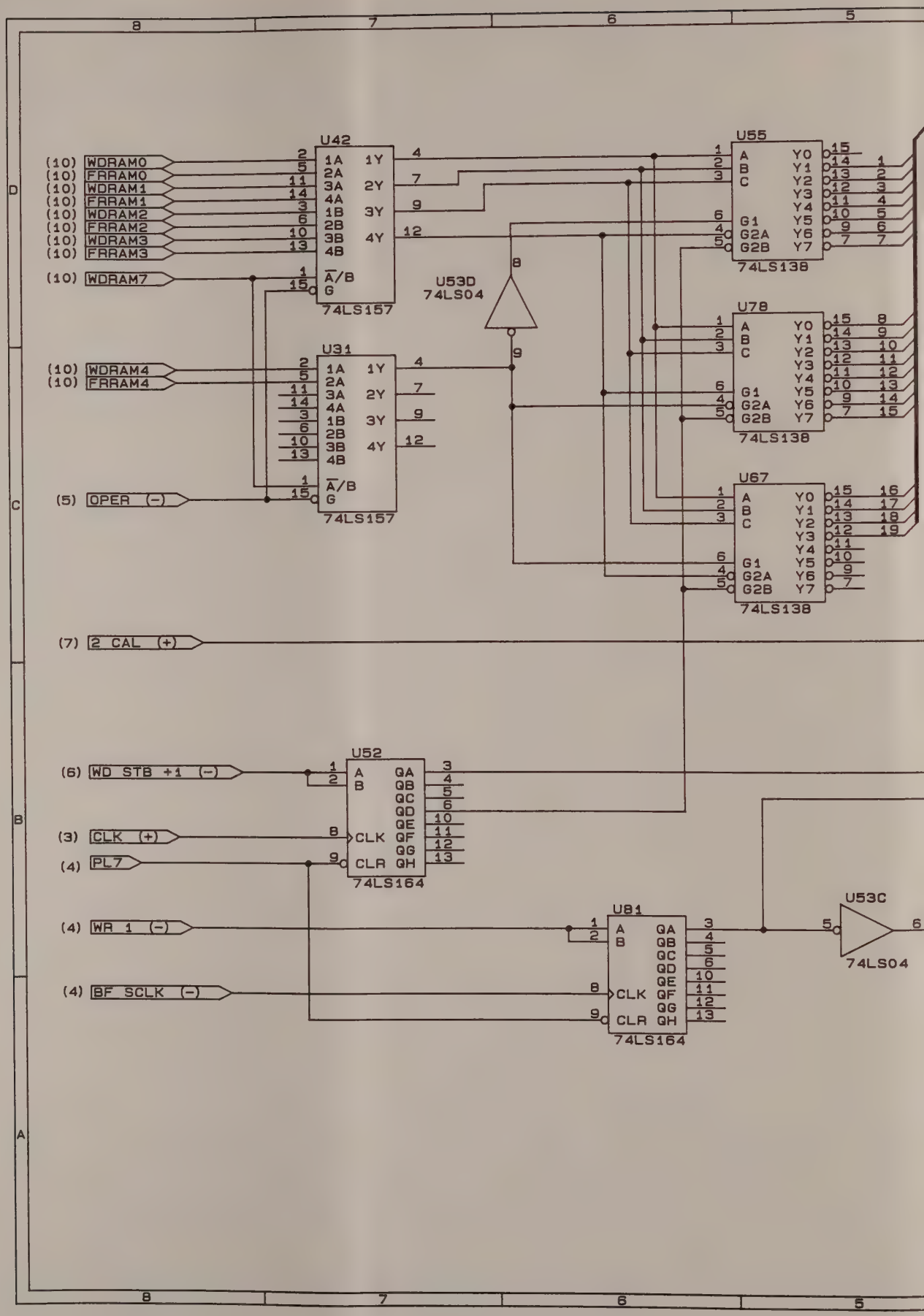


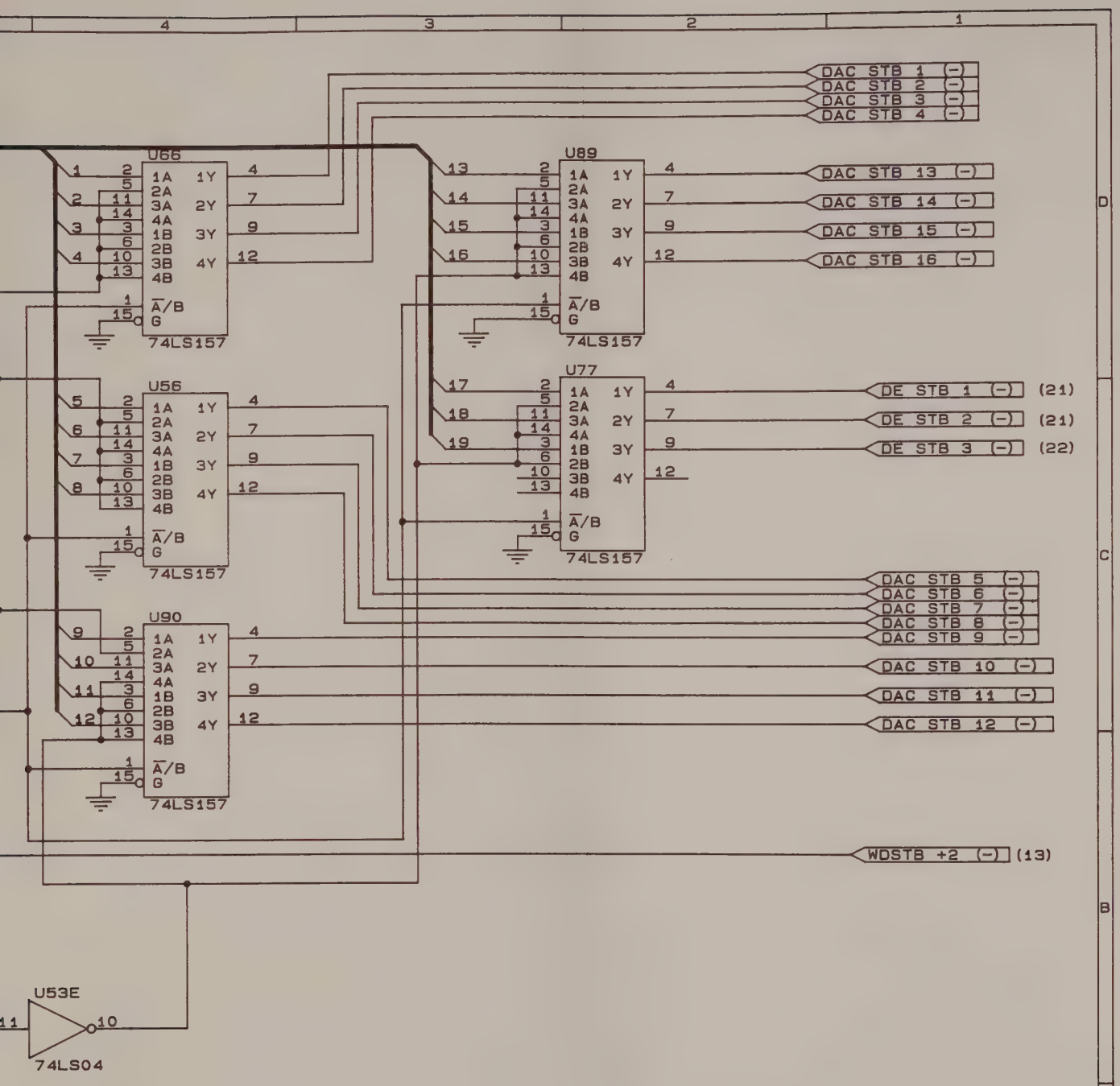
WORD COUNT RAM			
SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	20747	LD500-0989	—
		SHEET NO. 10 OF 22	


8
7
6
5
D
C
B
A
11-[0..15]
U10
FC0
FC1
FC2
FC3
FC4
FC5
FC6
FC7
D0 Q0
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
D7 Q7
11-0
11-1
11-2
11-3
11-4
11-5
11-6
11-7
(7) 1 OPER (-)
(12) WD STB +2 (-)
OC
CLK
74LS374
U11
FC8
FC9
FC10
FC11
(10) 1-WDRAM0
(10) 1-WDRAM1
(10) 1-WDRAM2
(10) 1-WDRAM3
11-8
11-9
11-10
11-11
11-12
11-13
11-14
11-15
74LS374
(5) MA/CD[0..15]
MA/CD[0..15]
U48
MA/CD0
MA/CD1
MA/CD2
MA/CD3
MA/CD4
MA/CD5
MA/CD6
MA/CD7
1A1 1Y1
1A2 1Y2
1A3 1Y3
1A4 1Y4
2A1 2Y1
2A2 2Y2
2A3 2Y3
2A4 2Y4
(7) 1 OPER (+)
1G
2G
74LS244
U22
MA/CD8
MA/CD9
MA/CD10
MA/CD11
MA/CD12
MA/CD13
MA/CD14
MA/CD15
74LS244
U79D
(4) WR 3 (-)
74LS32

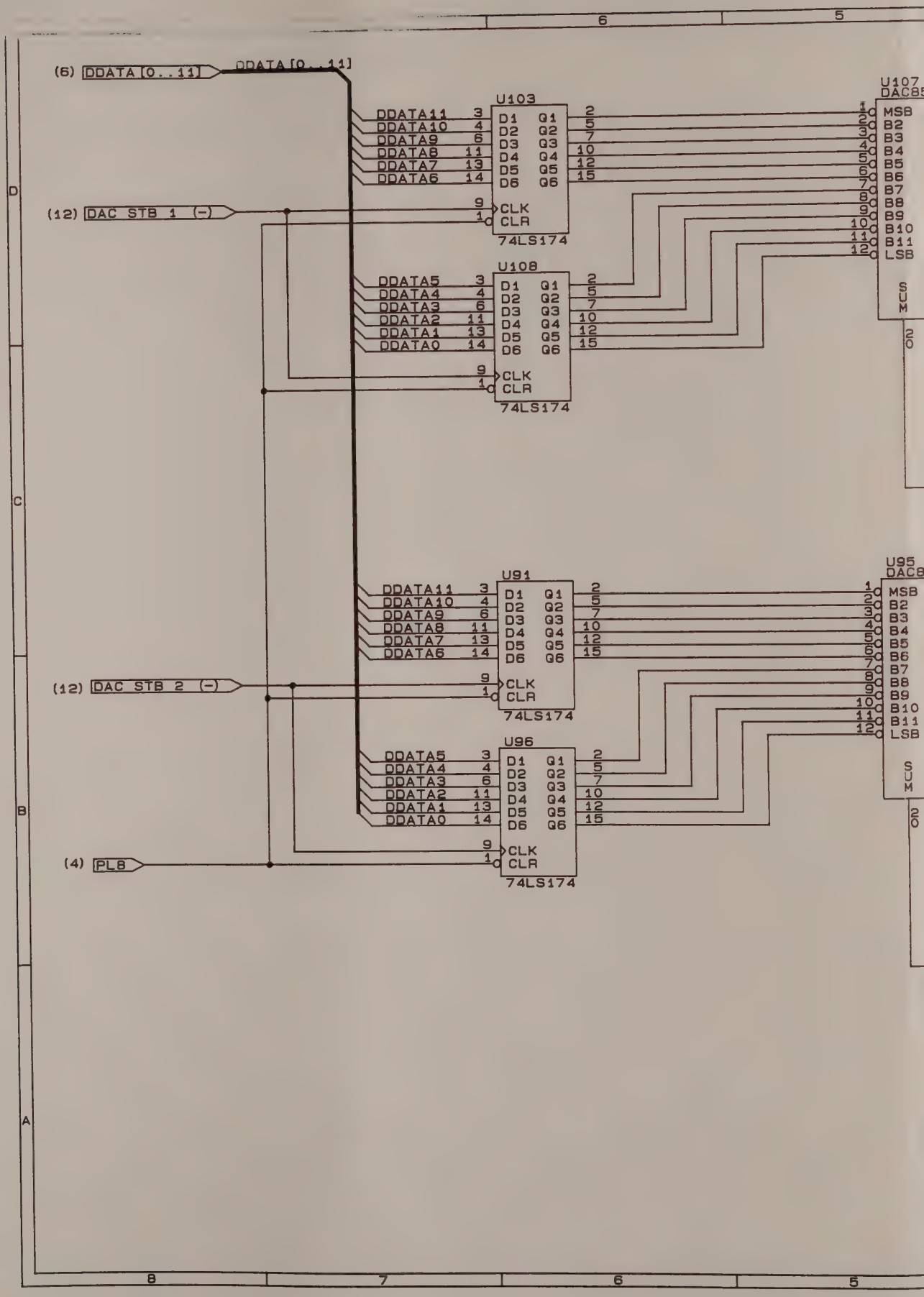


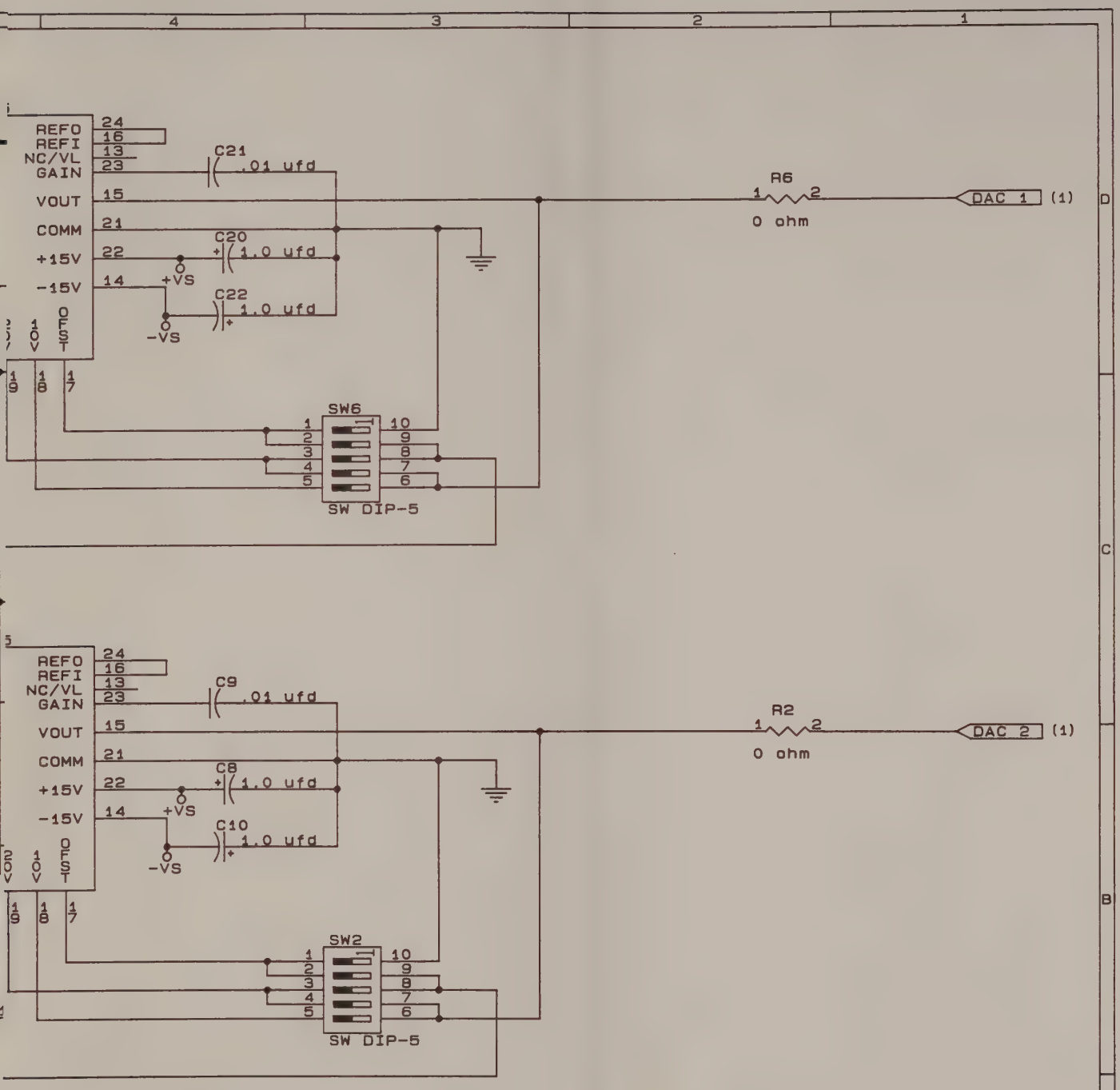
FRAME COUNT RAM			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 11 OF 22			


8
7
6
5
D
C
B
A
U42
74LS157
(10) WDRAM0
(10) FRRAM0
(10) WDRAM1
(10) FRRAM1
(10) WDRAM2
(10) FRRAM2
(10) WDRAM3
(10) FRRAM3
(10) WDRAM7
1A
2A
3A
4A
1B
2B
3B
4B
A/B
G
1Y
2Y
3Y
4Y
U53D
74LS04
U31
74LS157
(10) WDRAM4
(10) FRRAM4
(5) OPER (-)
U55
74LS138
U78
74LS138
U67
74LS138
A
B
C
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
(7) 2 CAL (+)
U52
74LS164
(6) WD STB +1 (-)
(3) CLK (+)
(4) PL7
A
B
CLK
CLR
QA
QB
QC
QD
QE
QF
QG
QH
U81
74LS164
(4) WR 1 (-)
(4) BF SCLK (-)
U53C
74LS04

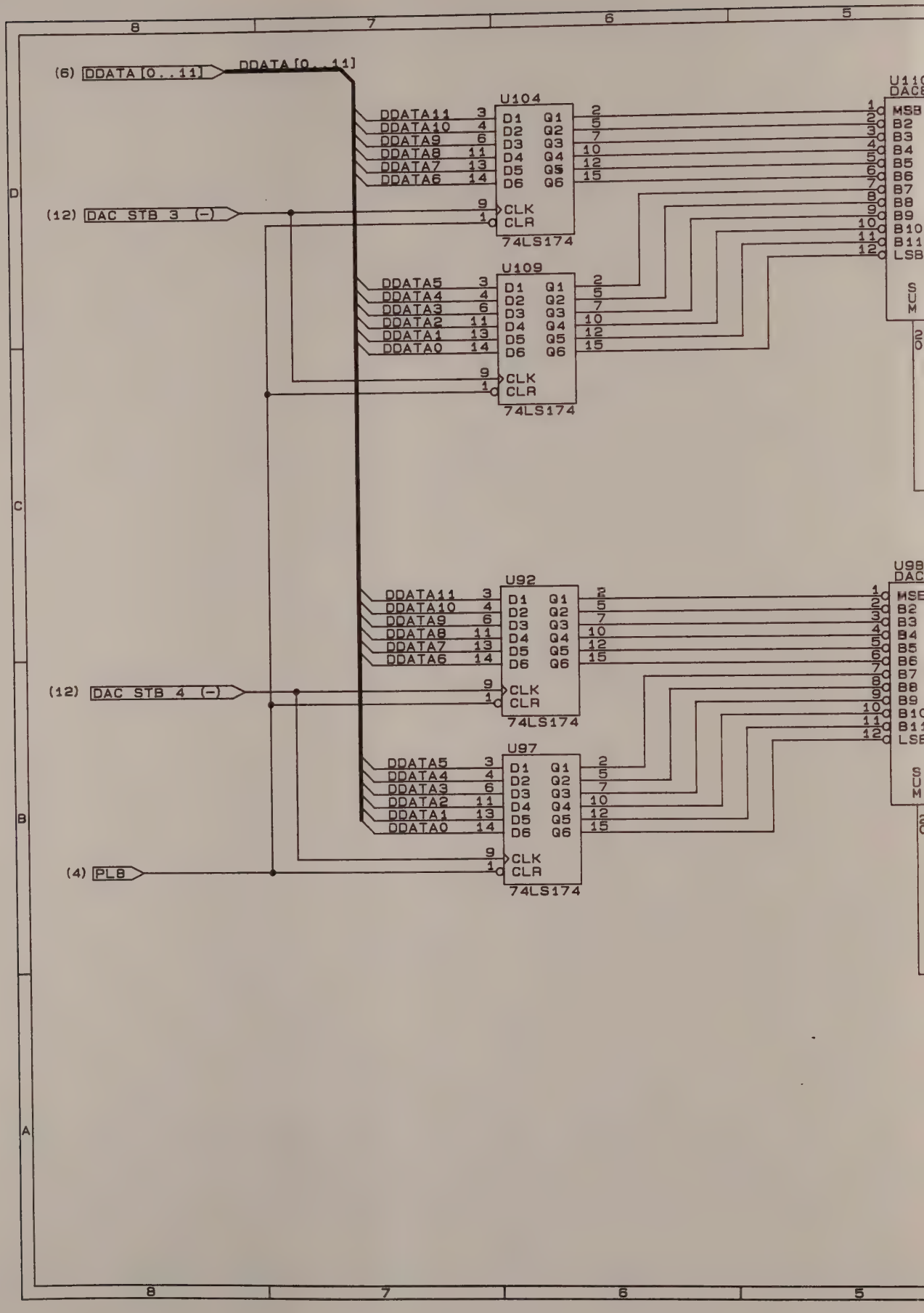


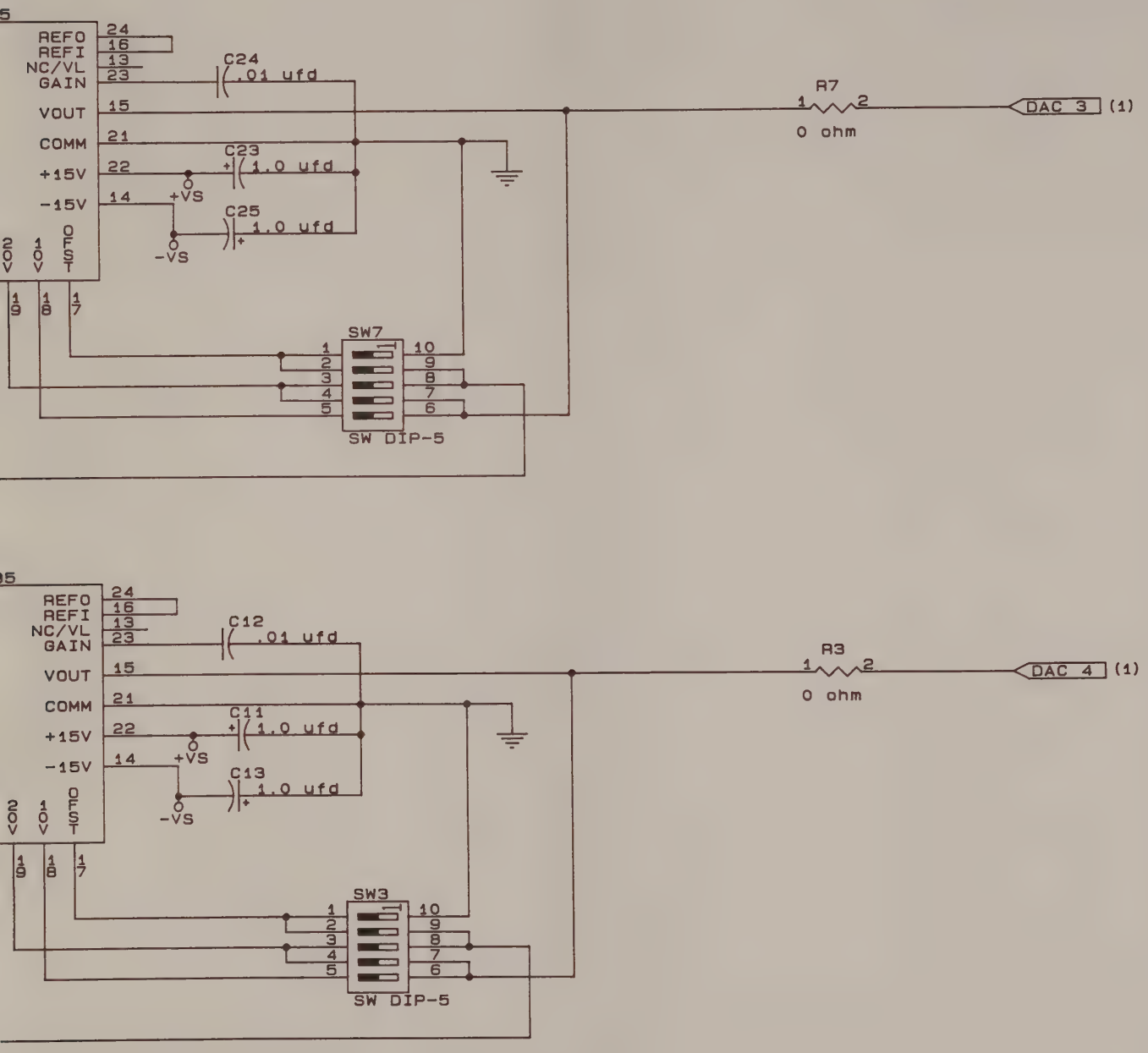
DAC AND DE STB GENERATION			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 12 OF 22			


(6) DDATA[0..11]
DDATA[0..11]
U103
DDATA11 3
DDATA10 4
DDATA9 6
DDATA8 11
DDATA7 13
DDATA6 14
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
2
5
7
10
12
15
9 CLK
1 CLR
74LS174
(12) DAC STB 1 (-)
U107
DAC85
MSB
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
LSB
SUM
U108
DDATA5 3
DDATA4 4
DDATA3 6
DDATA2 11
DDATA1 13
DDATA0 14
U91
U95
DAC8
(12) DAC STB 2 (-)
U96
(4) PL8
D
C
B
A
8
7
6
5

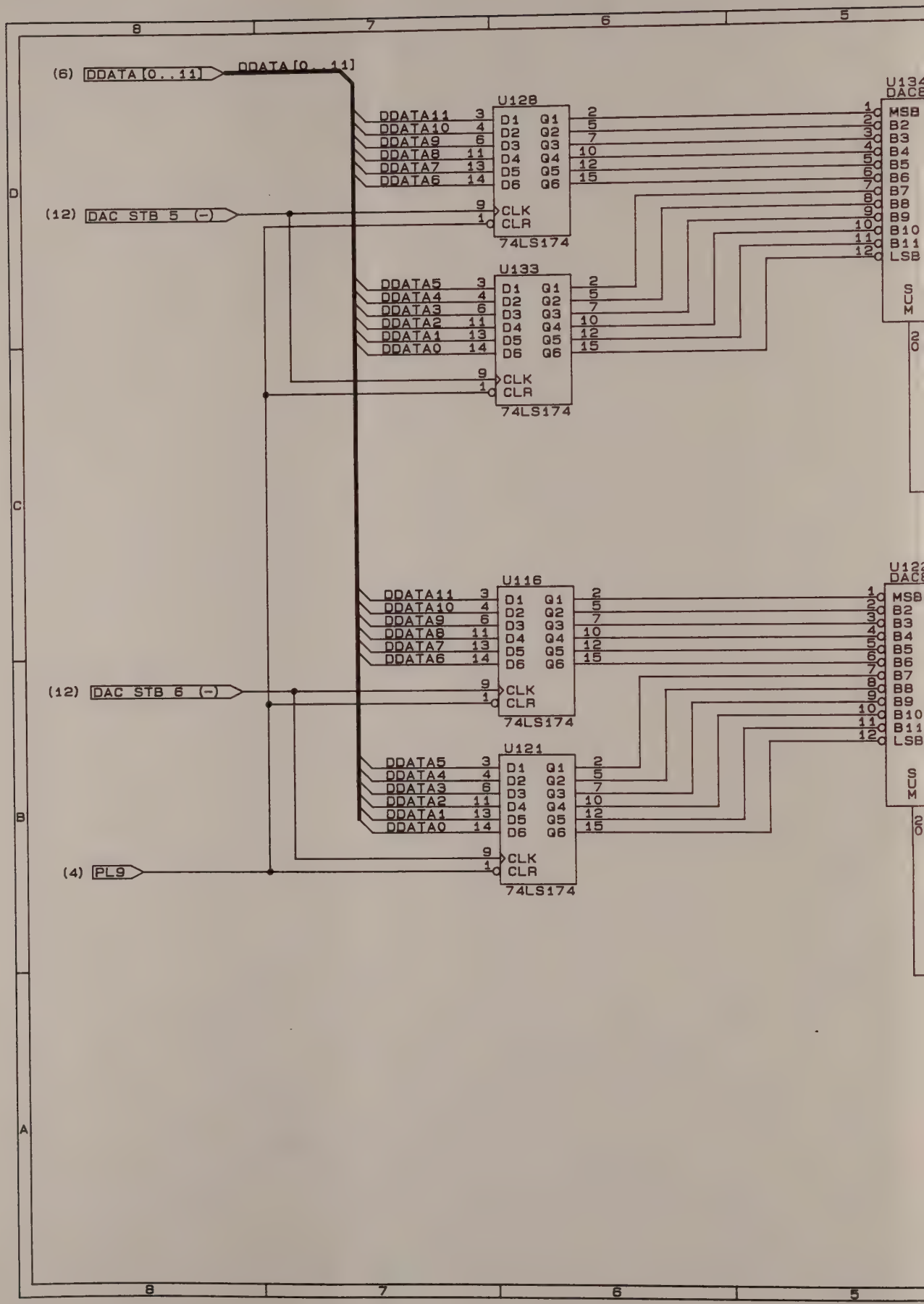


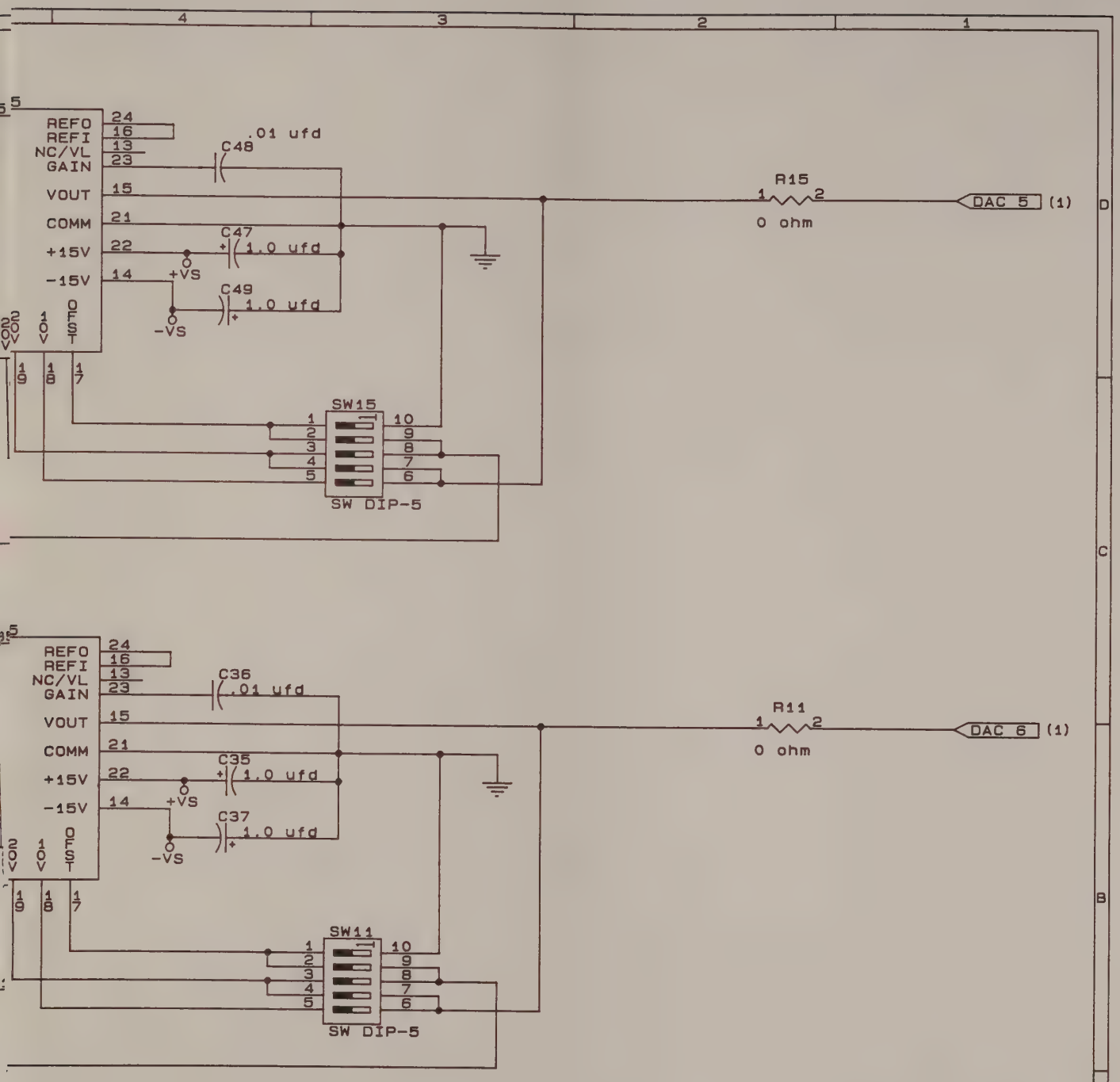
DAC 1 & 2 OUTPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 13 OF 22			


8
7
6
5
D
C
B
A
(6) DDATA [0..11]
DDATA [0..11]
U104
DDATA11 3
DDATA10 4
DDATA9 6
DDATA8 11
DDATA7 13
DDATA6 14
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
2
5
7
10
12
15
9 CLK
1 CLR
74LS174
(12) DAC STB 3 (-)
U109
DDATA5 3
DDATA4 4
DDATA3 6
DDATA2 11
DDATA1 13
DDATA0 14
U110
DAC
MSB
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
LSB
SUM
U92
U97
U98
(12) DAC STB 4 (-)
(4) PL8

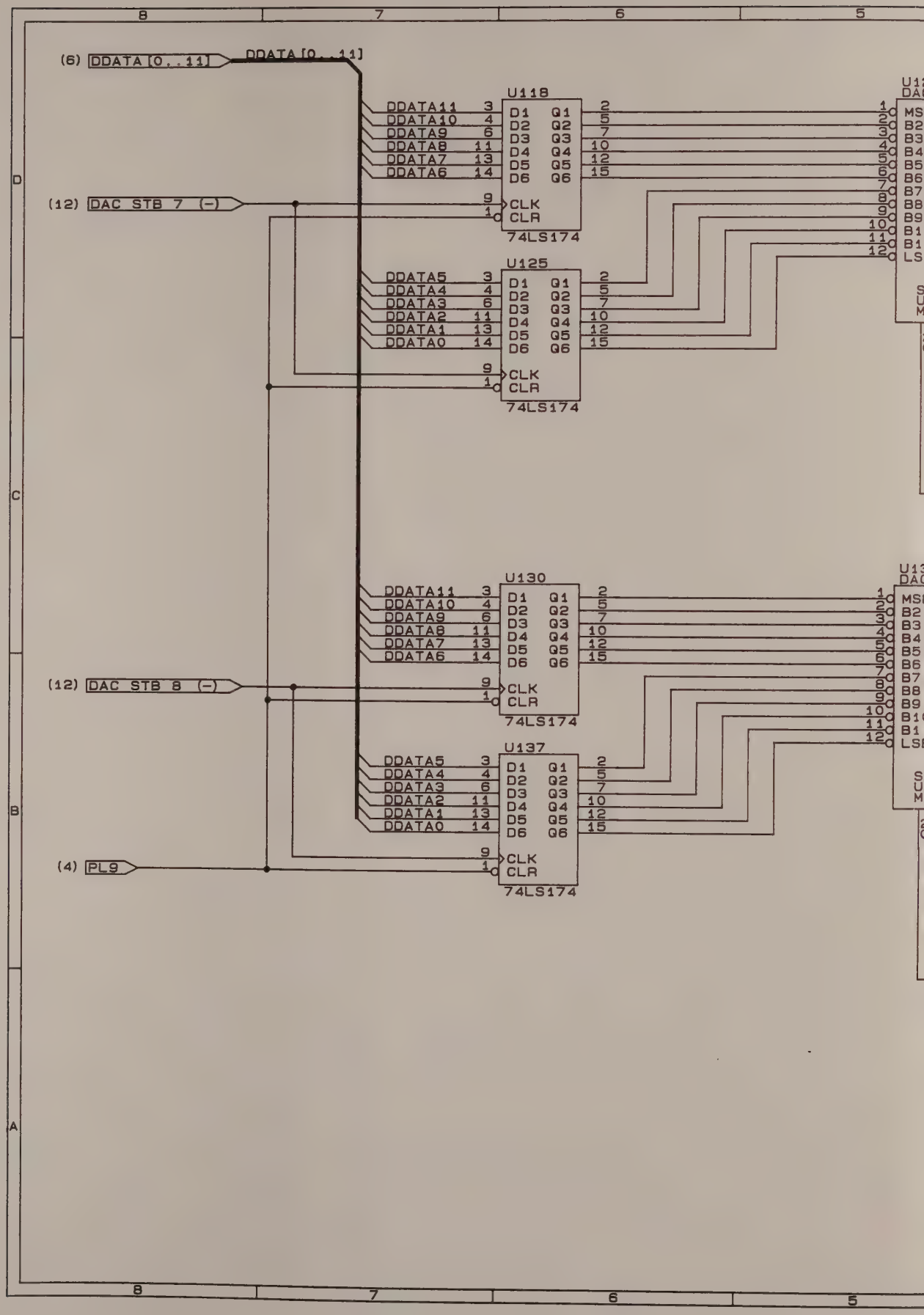


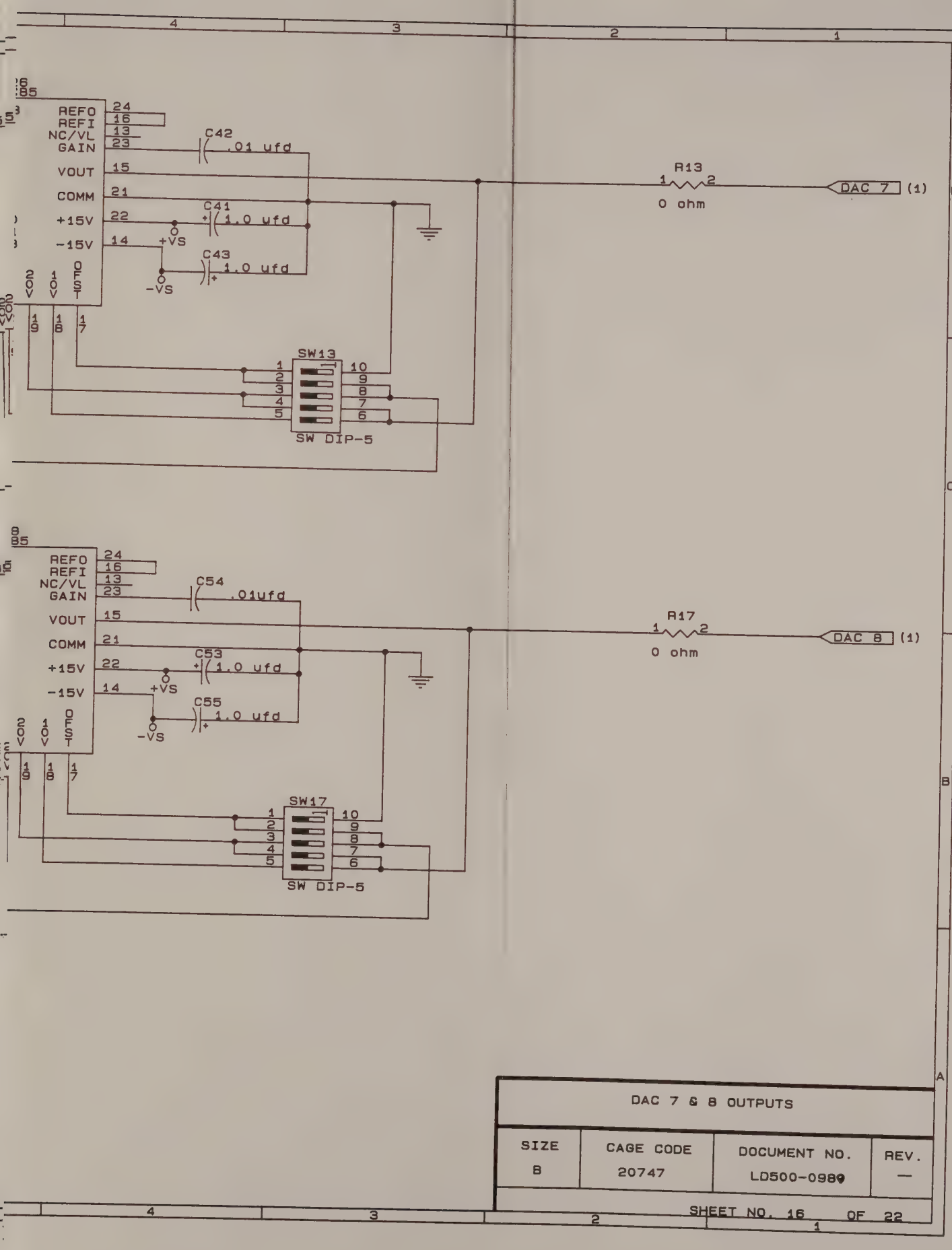
DAC 3 & 4 OUTPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
		SHEET NO. 14 OF 22	


8
7
6
5
D
C
B
A
(6) DDATA[0..11]
DDATA[0..11]
U128
DDATA11 3
DDATA10 4
DDATA9 6
DDATA8 11
DDATA7 13
DDATA6 14
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
2
5
7
10
12
15
(12) DAC STB 5 (-)
9 CLK
1 CLR
74LS174
U133
DDATA5 3
DDATA4 4
DDATA3 6
DDATA2 11
DDATA1 13
DDATA0 14
U134
DACB
MSB
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
LSB
SUM
U116
(12) DAC STB 6 (-)
U121
(4) PL9
U122
DACS

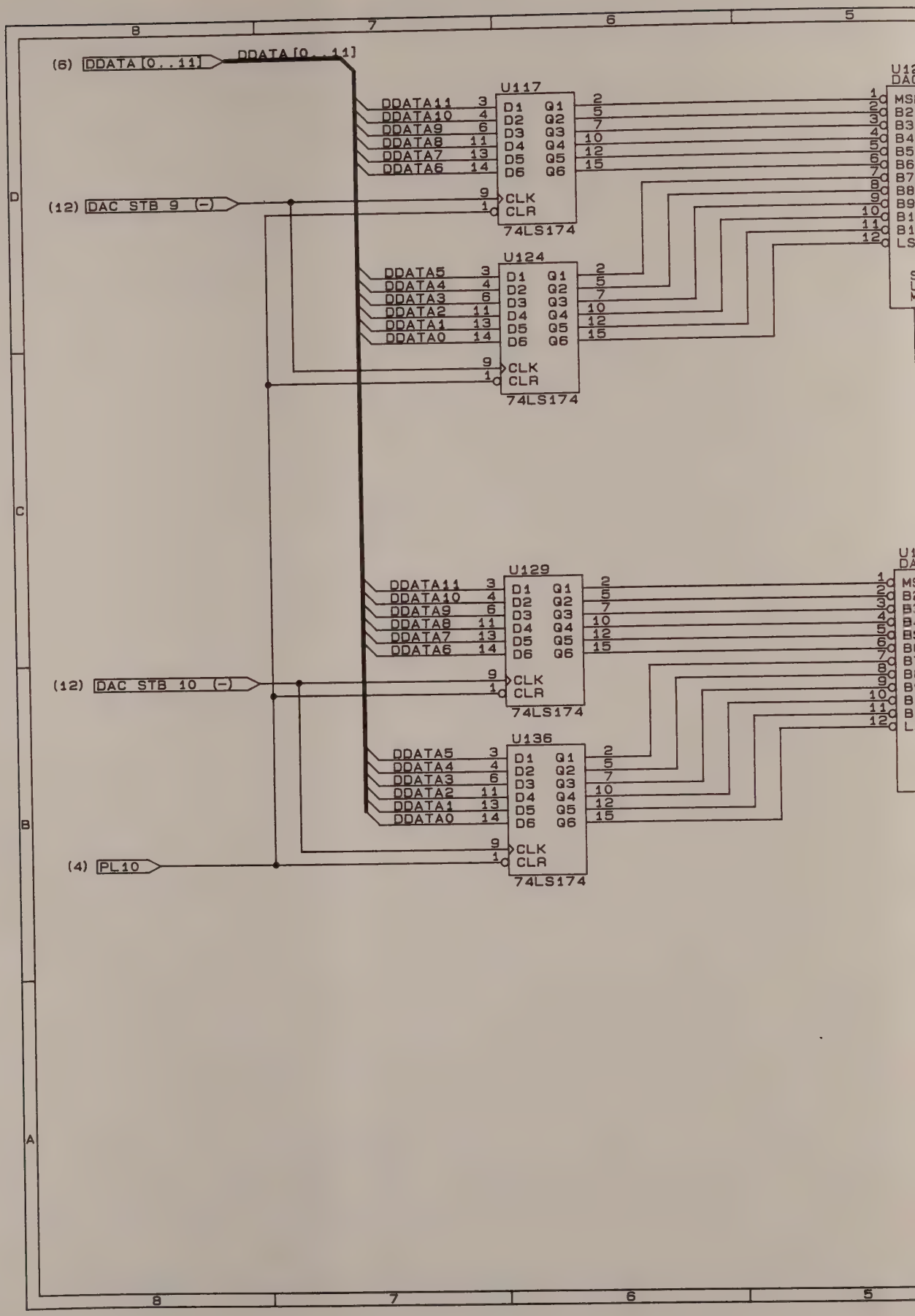


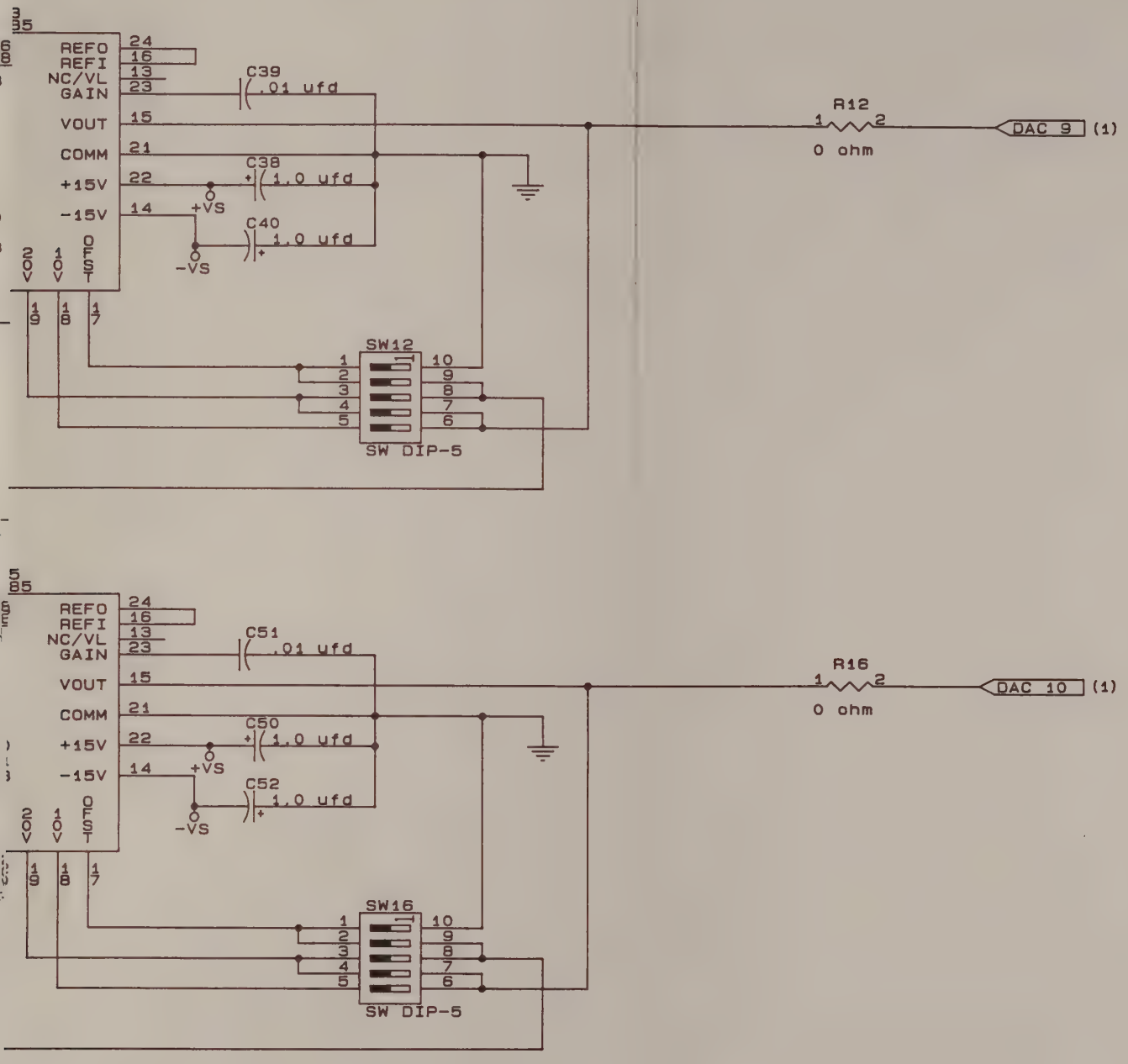
DAC 5 & 6 OUTPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 15 OF 22			


(6) DDATA[0..11]
DDATA[0..11]
U118
DDATA11 3
DDATA10 4
DDATA9 6
DDATA8 11
DDATA7 13
DDATA6 14
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
2
5
7
10
12
15
(12) DAC STB 7 (-)
9 CLK
1 CLR
74LS174
U125
DDATA5 3
DDATA4 4
DDATA3 6
DDATA2 11
DDATA1 13
DDATA0 14
U130
(12) DAC STB 8 (-)
U137
(4) PL9
MS
B2
B3
B4
B5
B6
B7
B8
B9
B1
B1
LS
1
2
3
4
5
6
7
8
9
10
11
12

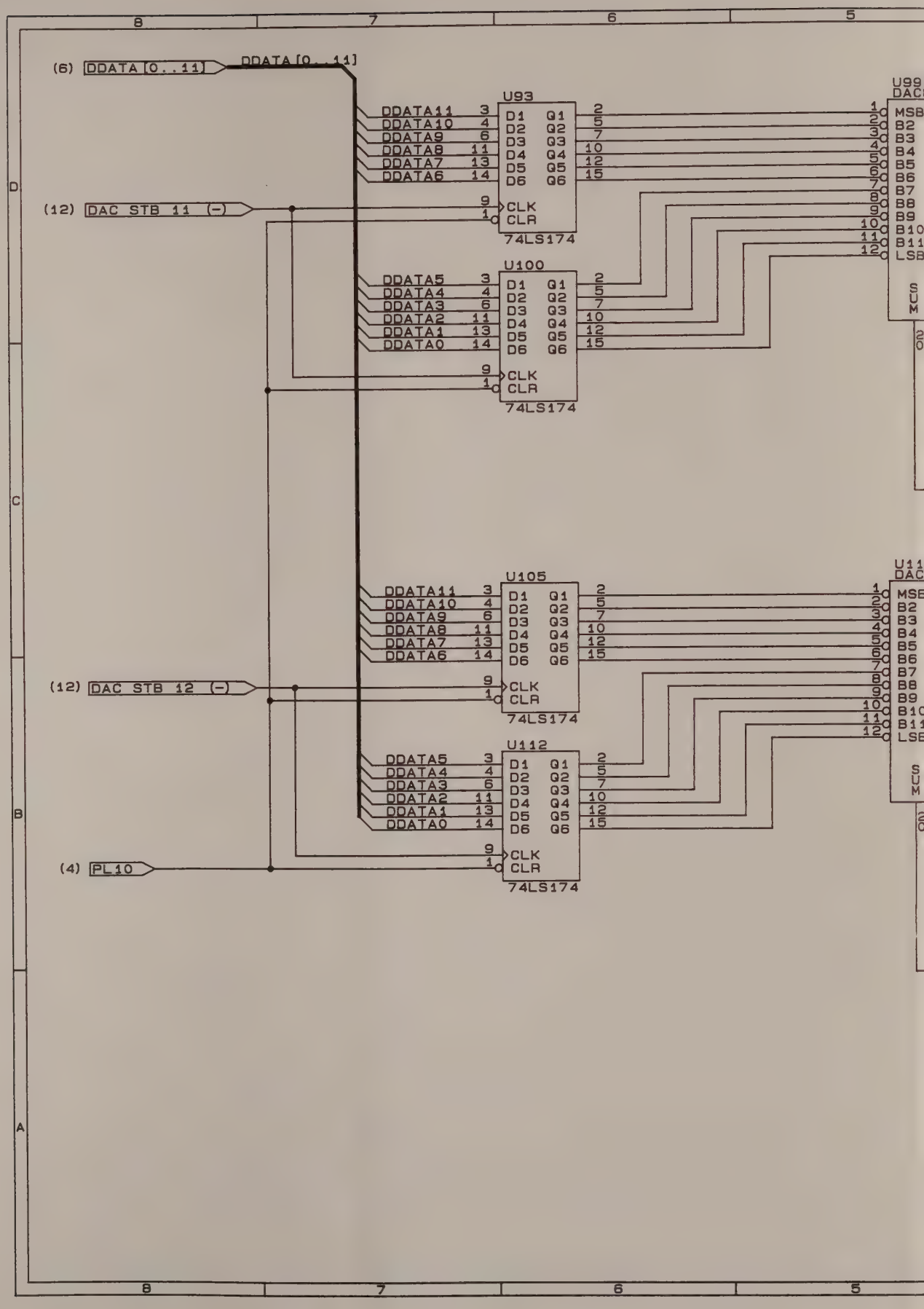


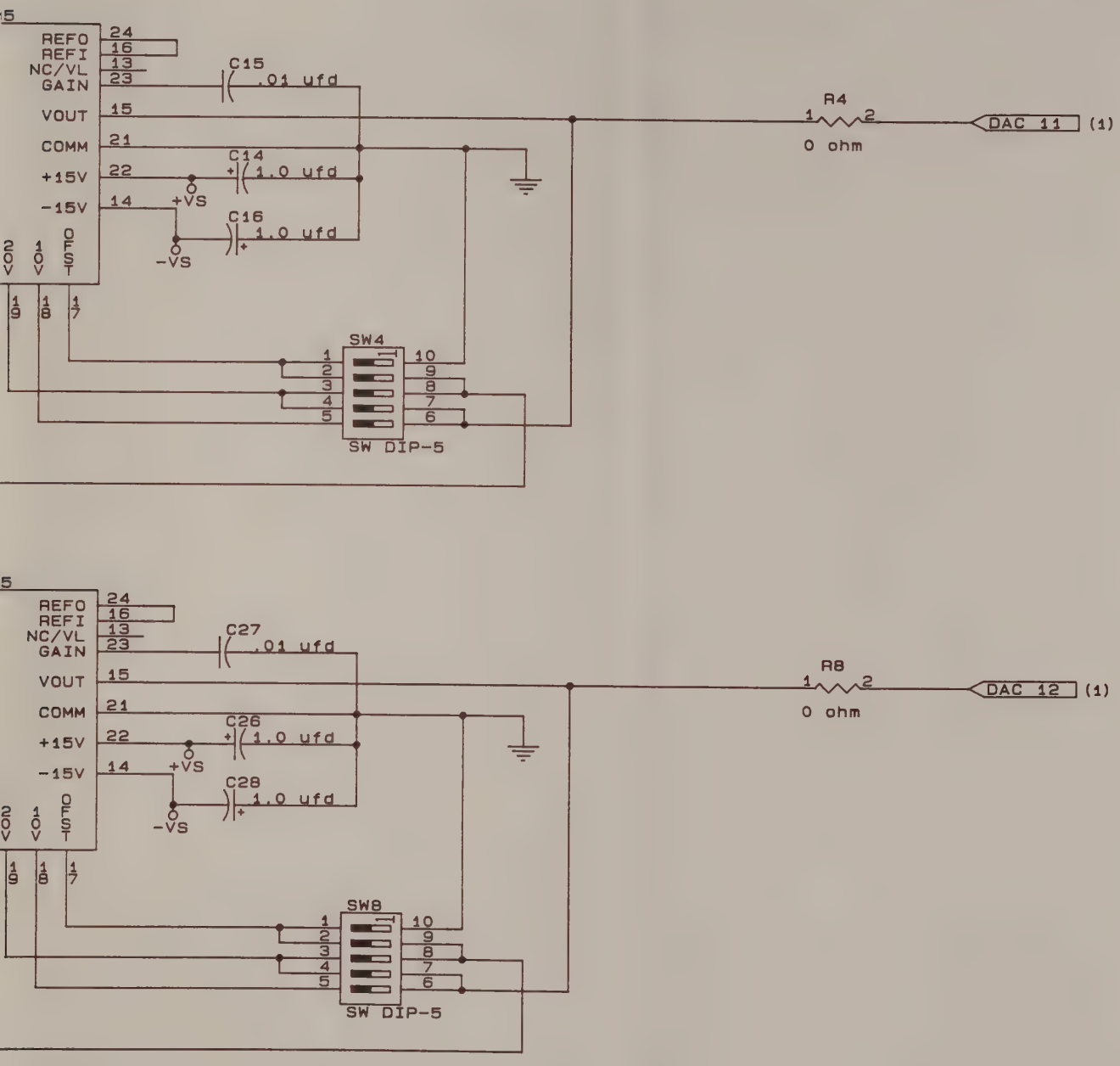
DAC 7 & 8 OUTPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 16 OF 22			


(6) DDATA [0..11]
DDATA [0..11]
U117
DDATA11 3
DDATA10 4
DDATA9 6
DDATA8 11
DDATA7 13
DDATA6 14
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
2
5
7
10
12
15
9 CLK
1 CLR
74LS174
(12) DAC STB 9 (-)
U124
DDATA5 3
DDATA4 4
DDATA3 6
DDATA2 11
DDATA1 13
DDATA0 14
74LS174
U129
DDATA11 3
DDATA10 4
DDATA9 6
DDATA8 11
DDATA7 13
DDATA6 14
74LS174
(12) DAC STB 10 (-)
U136
DDATA5 3
DDATA4 4
DDATA3 6
DDATA2 11
DDATA1 13
DDATA0 14
74LS174
(4) PL10
D
C
B
A
8
7
6
5

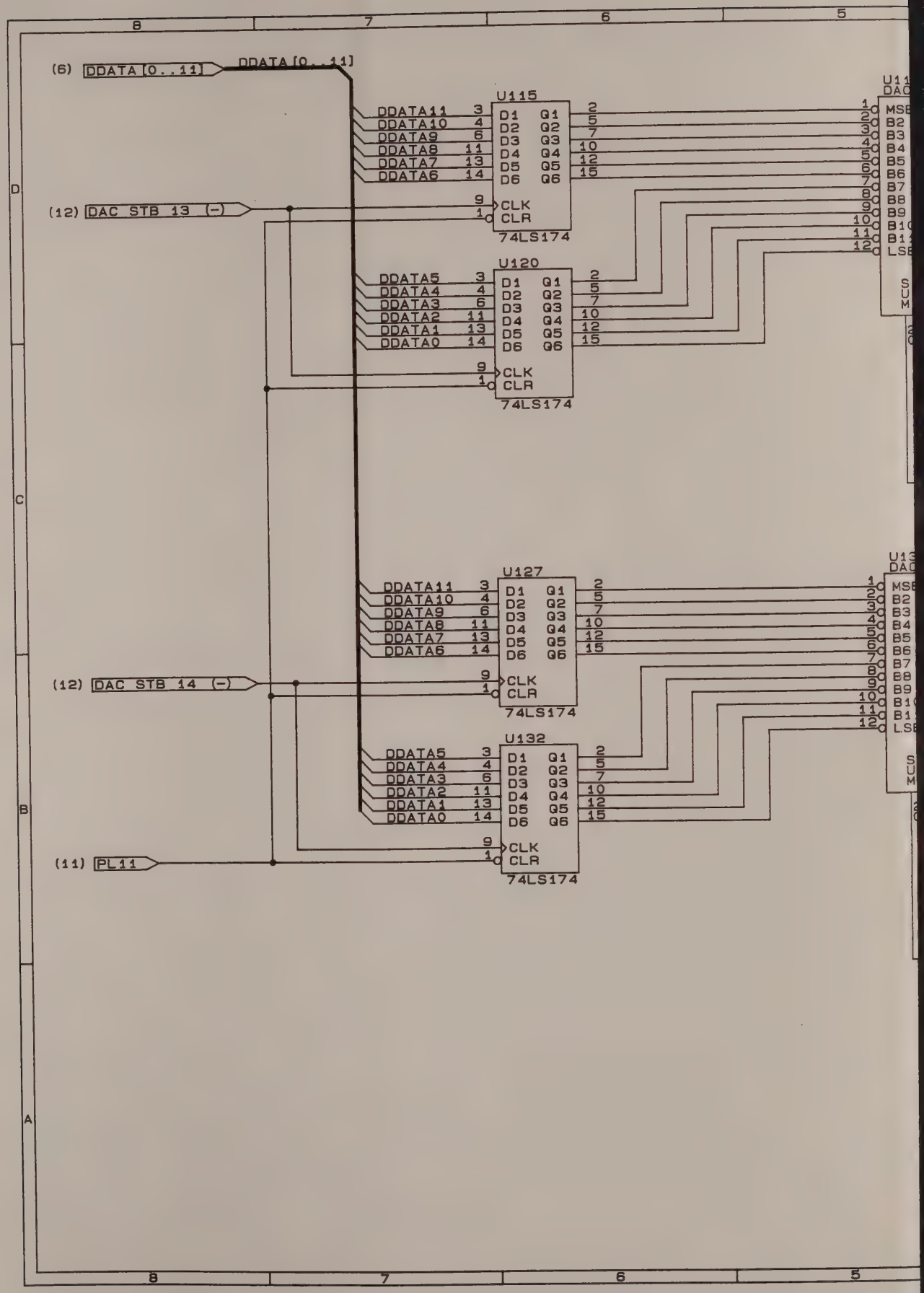


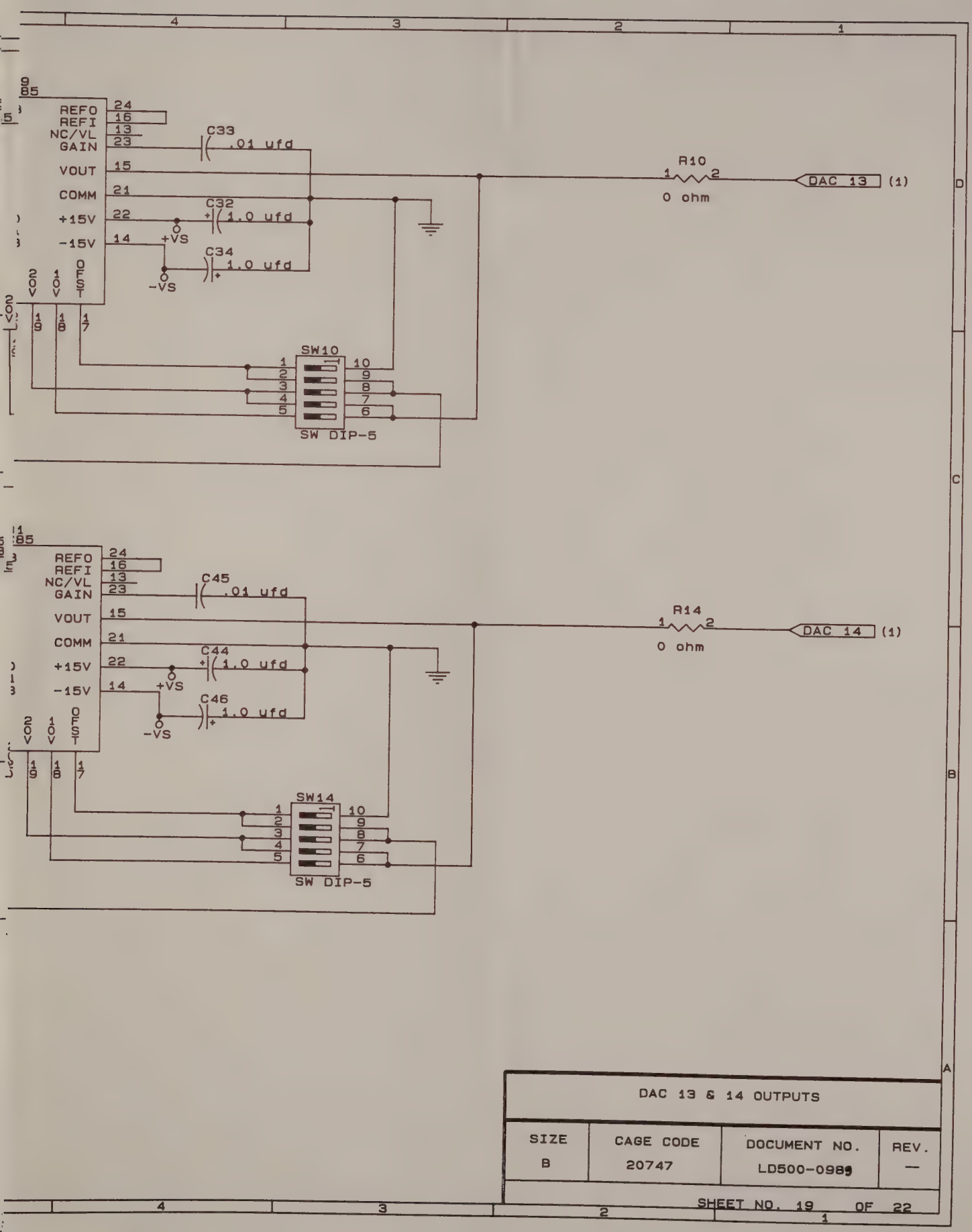
DAC 9 & 10 OUTPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 17 OF 22			


(6) DDATA [0..11]
DDATA [0..11]
(12) DAC STB 11 (-)
(12) DAC STB 12 (-)
(4) PL10
U93
U100
U105
U112
74LS174
DDATA11
DDATA10
DDATA9
DDATA8
DDATA7
DDATA6
DDATA5
DDATA4
DDATA3
DDATA2
DDATA1
DDATA0
D1 D2 D3 D4 D5 D6
Q1 Q2 Q3 Q4 Q5 Q6
CLK
CLR
MSB
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
LSB

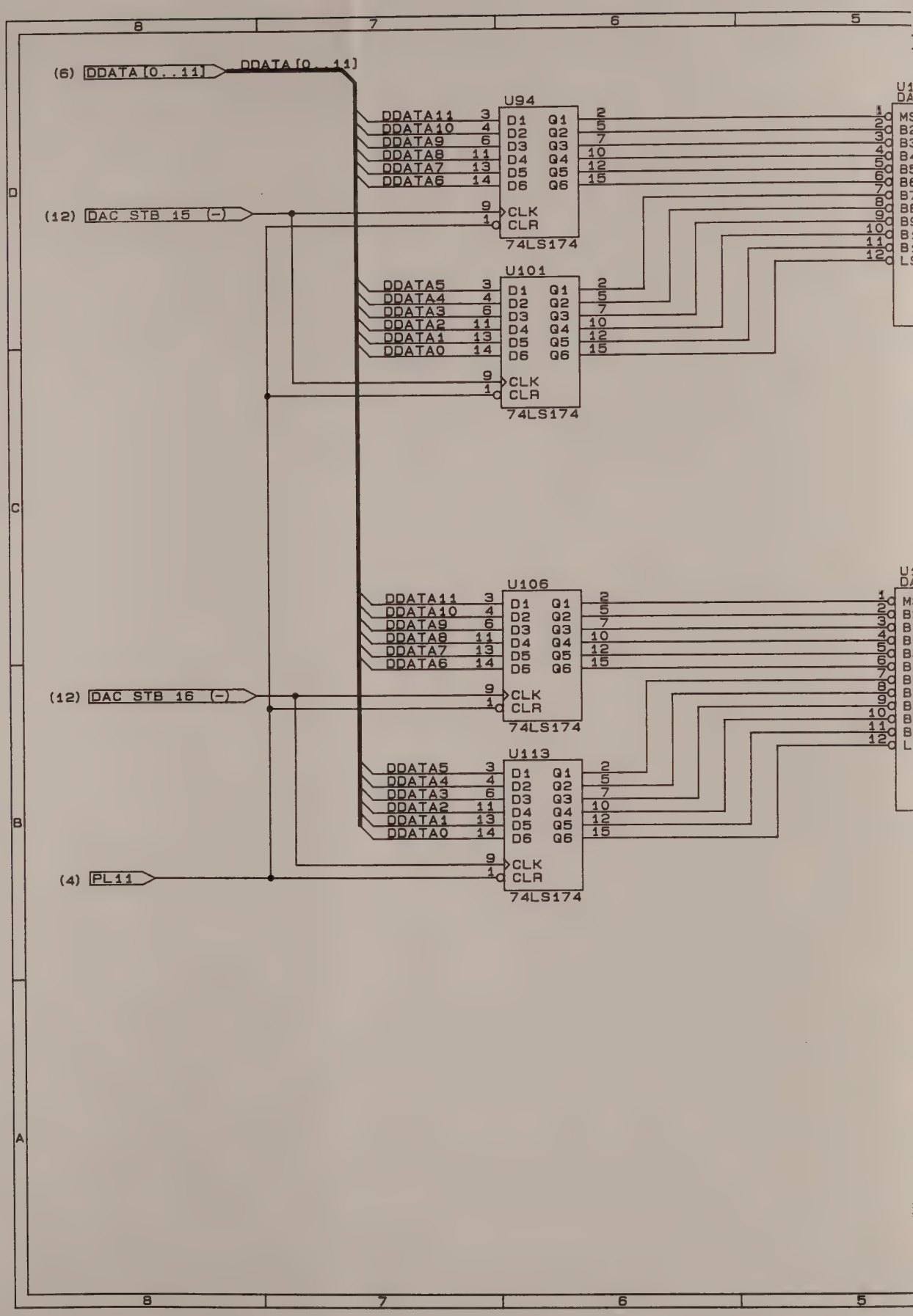


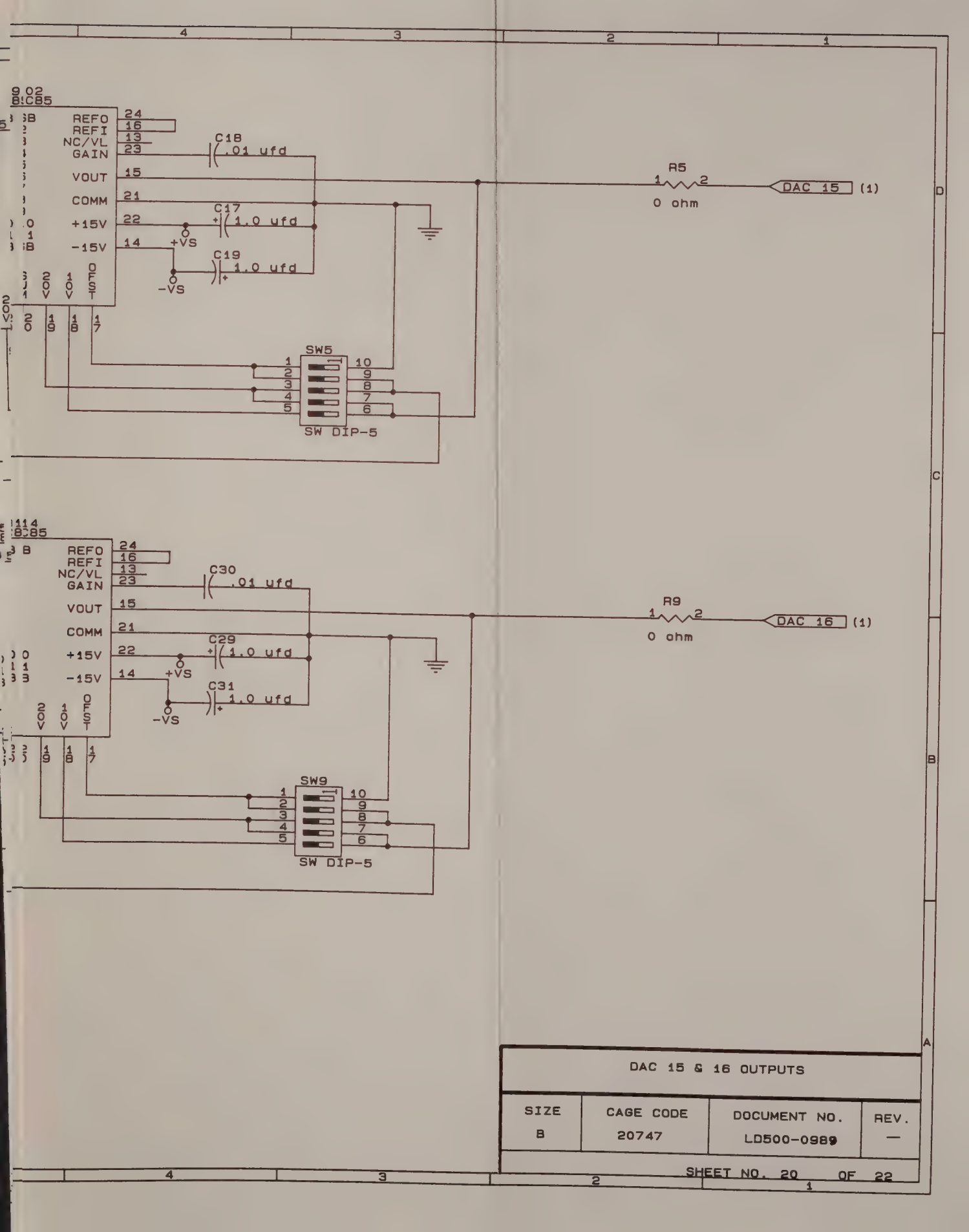
DAC 11 & 12 OUTPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 18 OF 22			


(6) DDATA [0..11]
DDATA [0..11]
U115
DDATA11 3
DDATA10 4
DDATA9 6
DDATA8 11
DDATA7 13
DDATA6 14
D1 Q1 2
D2 Q2 5
D3 Q3 7
D4 Q4 10
D5 Q5 12
D6 Q6 15
(12) DAC STB 13 (-)
9 CLK
1 CLR
74LS174
U120
DDATA5 3
DDATA4 4
DDATA3 6
DDATA2 11
DDATA1 13
DDATA0 14
D1 Q1 2
D2 Q2 5
D3 Q3 7
D4 Q4 10
D5 Q5 12
D6 Q6 15
9 CLK
1 CLR
74LS174
U127
DDATA11 3
DDATA10 4
DDATA9 6
DDATA8 11
DDATA7 13
DDATA6 14
D1 Q1 2
D2 Q2 5
D3 Q3 7
D4 Q4 10
D5 Q5 12
D6 Q6 15
(12) DAC STB 14 (-)
9 CLK
1 CLR
74LS174
U132
DDATA5 3
DDATA4 4
DDATA3 6
DDATA2 11
DDATA1 13
DDATA0 14
D1 Q1 2
D2 Q2 5
D3 Q3 7
D4 Q4 10
D5 Q5 12
D6 Q6 15
(11) PL11
9 CLK
1 CLR
74LS174
8
7
6
5
D
C
B
A

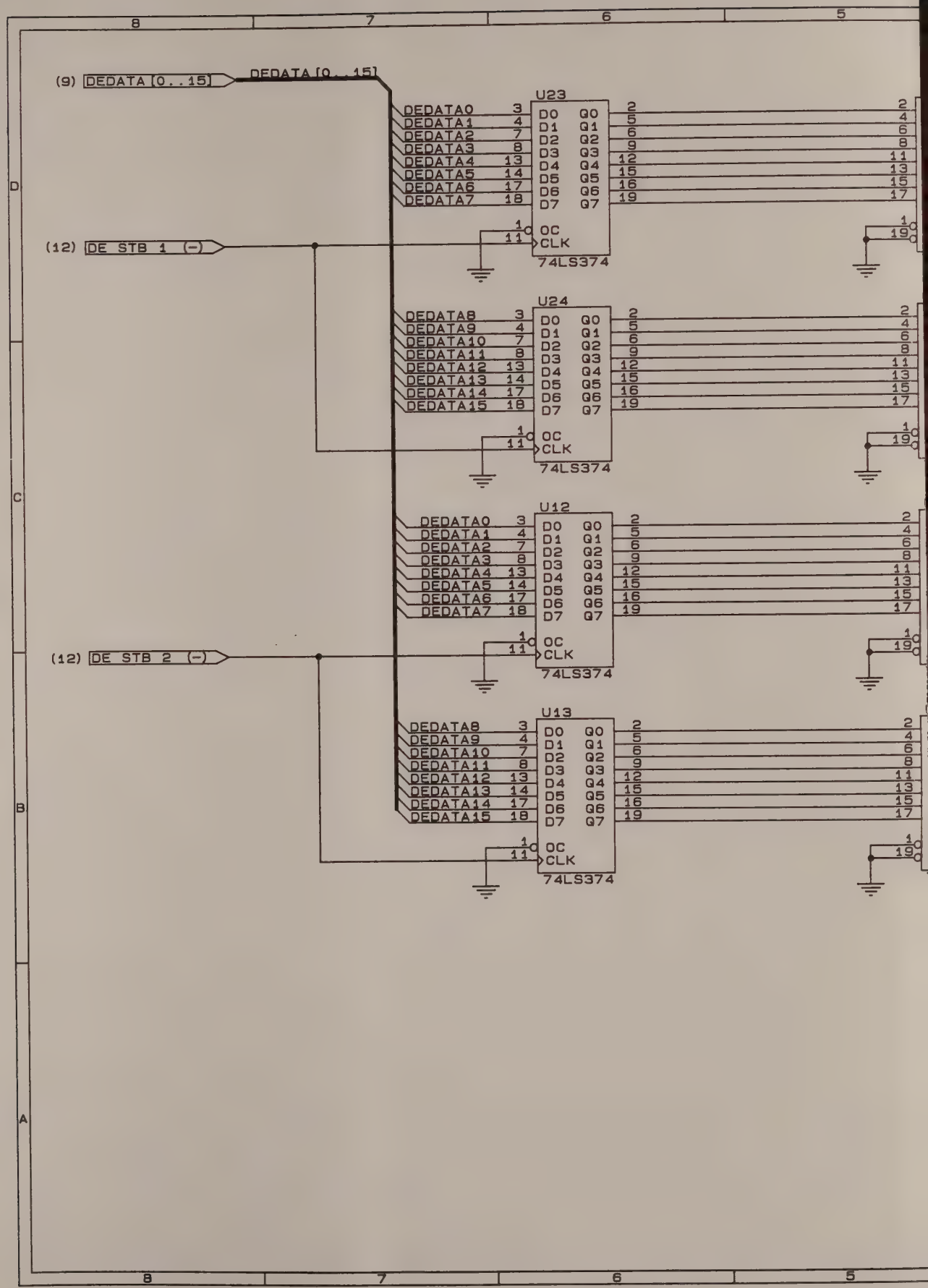
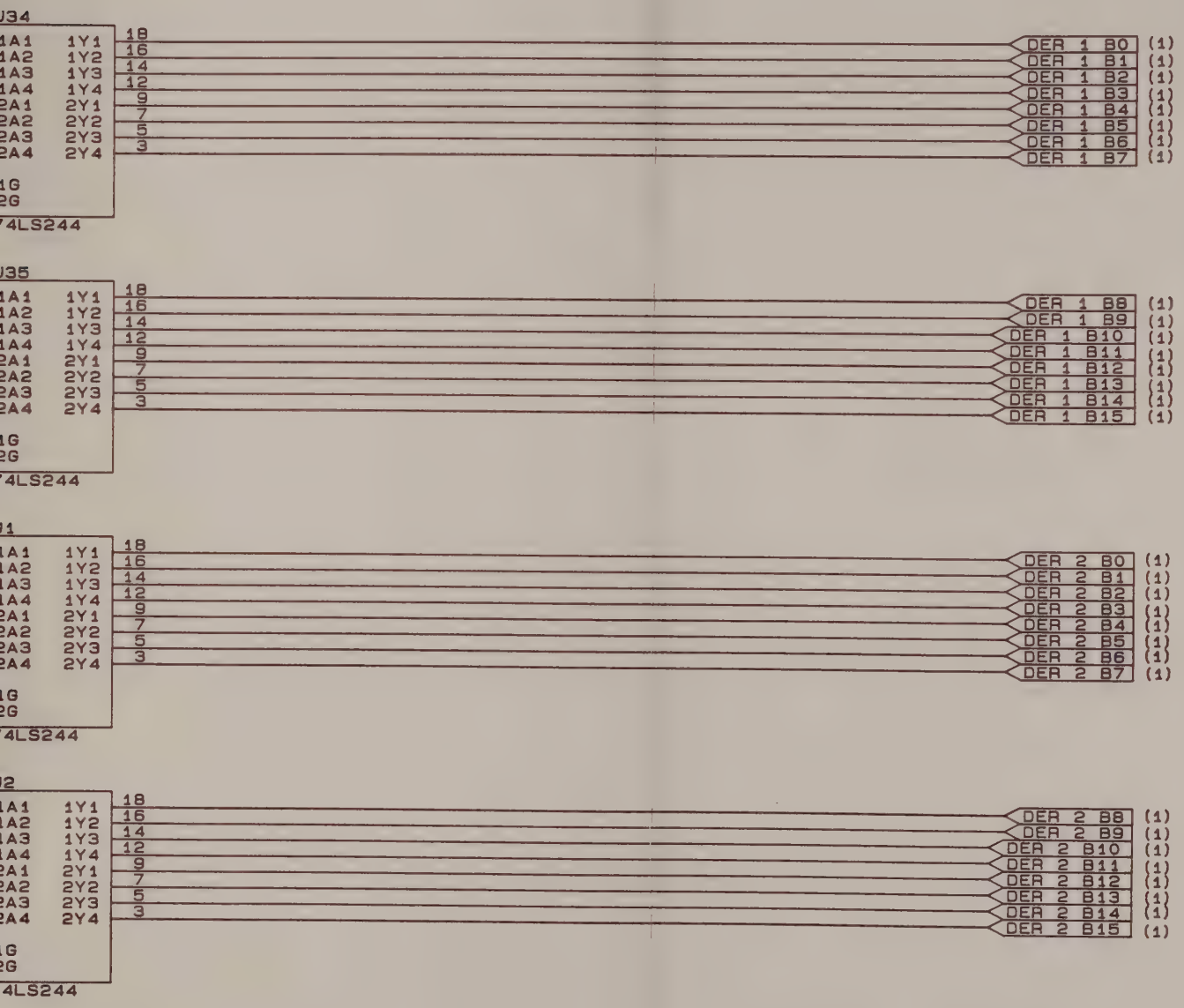


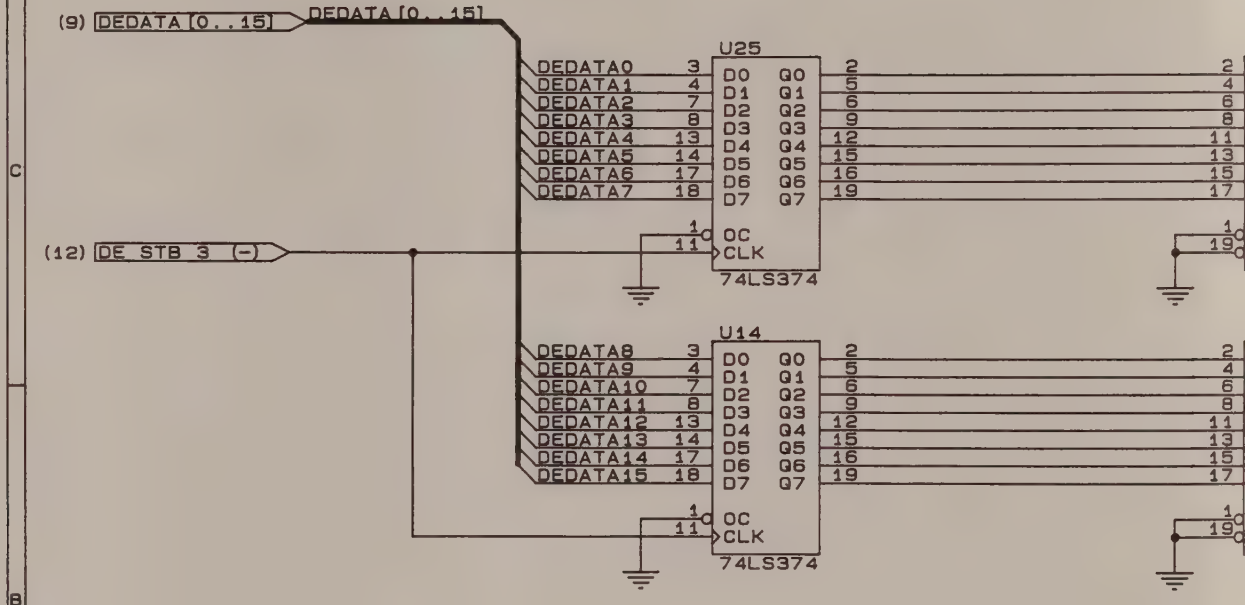
DAC 13 & 14 OUTPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 19 OF 22			

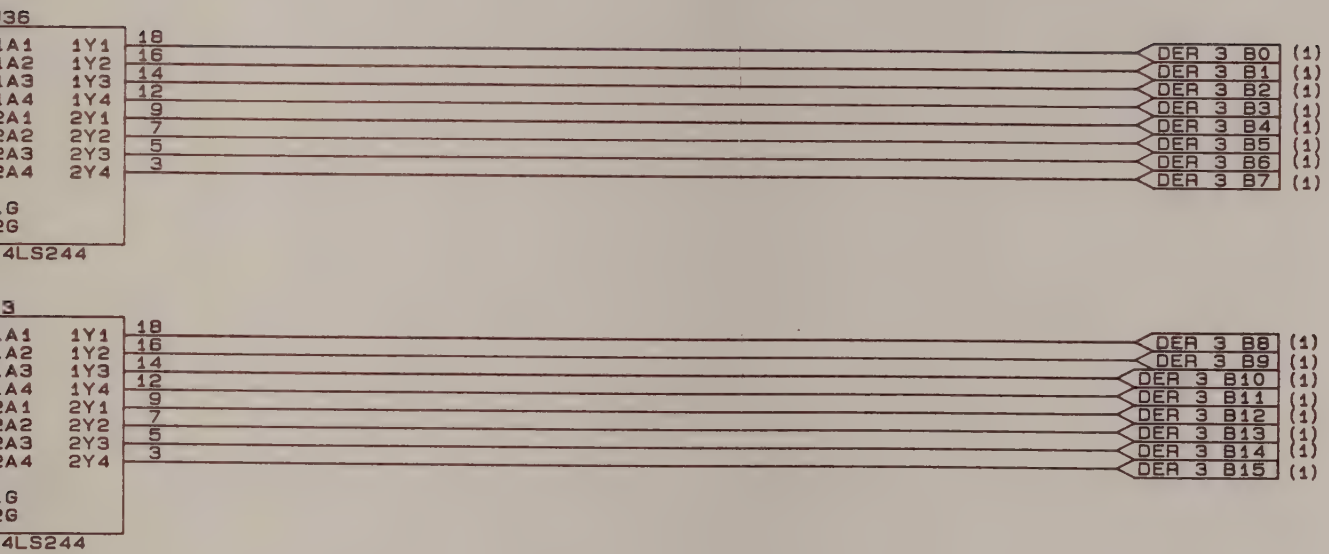

8
7
6
5
D
C
B
A
(6) DDATA[0..11]
DDATA[0..11]
U94
DDATA11 3
DDATA10 4
DDATA9 6
DDATA8 11
DDATA7 13
DDATA6 14
D1 Q1 2
D2 Q2 5
D3 Q3 7
D4 Q4 10
D5 Q5 12
D6 Q6 15
(12) DAC STB 15 (-)
9 CLK
1 CLR
74LS174
U101
DDATA5 3
DDATA4 4
DDATA3 6
DDATA2 11
DDATA1 13
DDATA0 14
D1 Q1 2
D2 Q2 5
D3 Q3 7
D4 Q4 10
D5 Q5 12
D6 Q6 15
9 CLK
1 CLR
74LS174
U106
DDATA11 3
DDATA10 4
DDATA9 6
DDATA8 11
DDATA7 13
DDATA6 14
D1 Q1 2
D2 Q2 5
D3 Q3 7
D4 Q4 10
D5 Q5 12
D6 Q6 15
(12) DAC STB 16 (-)
9 CLK
1 CLR
74LS174
U113
DDATA5 3
DDATA4 4
DDATA3 6
DDATA2 11
DDATA1 13
DDATA0 14
D1 Q1 2
D2 Q2 5
D3 Q3 7
D4 Q4 10
D5 Q5 12
D6 Q6 15
(4) PL11
9 CLK
1 CLR
74LS174



DAC 15 & 16 OUTPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 20 OF 22			


8
7
6
5
D
C
B
A
(9) DEDATA [0..15]
DEDATA [0..15]
(12) DE STB 1 (-)
(12) DE STB 2 (-)
U23
U24
U12
U13
DEDATA0
DEDATA1
DEDATA2
DEDATA3
DEDATA4
DEDATA5
DEDATA6
DEDATA7
DEDATA8
DEDATA9
DEDATA10
DEDATA11
DEDATA12
DEDATA13
DEDATA14
DEDATA15
D0 D1 D2 D3 D4 D5 D6 D7
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
OC
CLK
74LS374

DER 1 & 2 OUTPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 21 OF 22			


(9) DEDATA[0..15]
DEDATA[0..15]
(12) DE_STB_3_(-)
U25
DEDATA0 3
DEDATA1 4
DEDATA2 7
DEDATA3 8
DEDATA4 13
DEDATA5 14
DEDATA6 17
DEDATA7 18
D0 Q0
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
D7 Q7
2 2
5 4
6 6
9 8
12 11
15 13
16 15
19 17
1 OC
11 CLK
74LS374
U14
DEDATA8 3
DEDATA9 4
DEDATA10 7
DEDATA11 8
DEDATA12 13
DEDATA13 14
DEDATA14 17
DEDATA15 18
D0 Q0
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
D7 Q7
2 2
5 4
6 6
9 8
12 11
15 13
16 15
19 17
1 OC
11 CLK
74LS374



DER 3 OUTPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0989	REV. —
SHEET NO. 22 OF 22			

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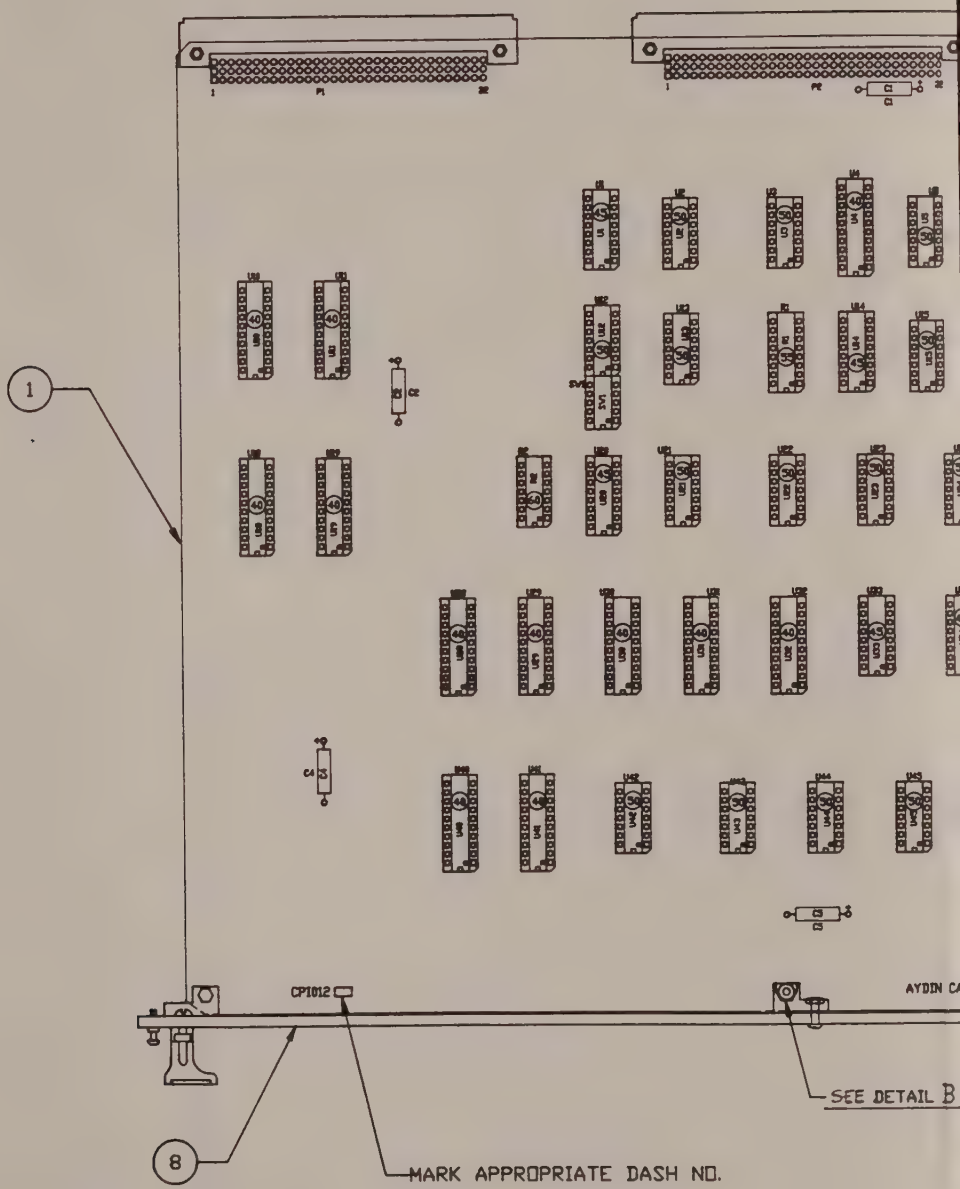
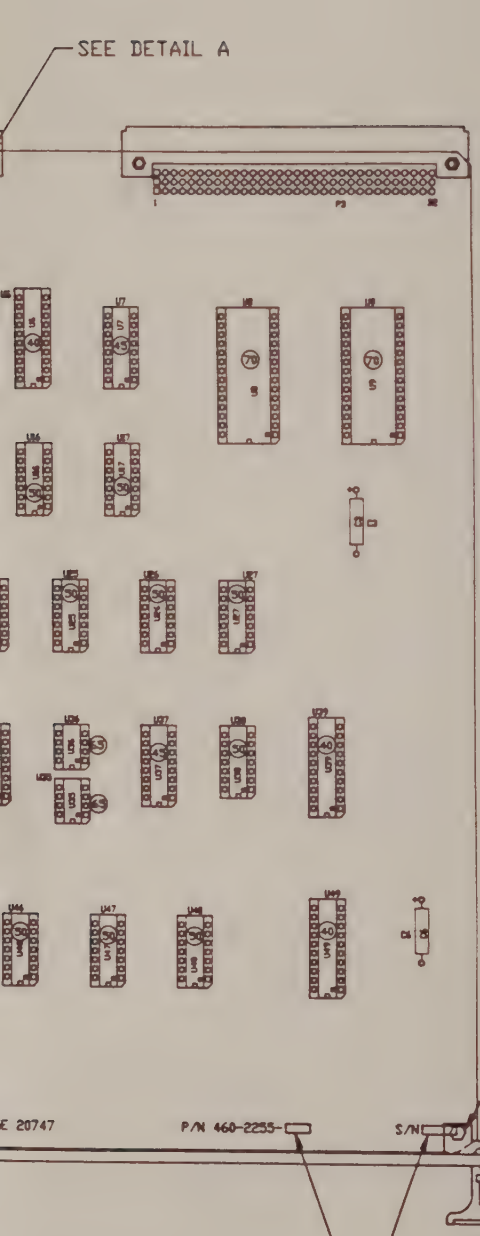
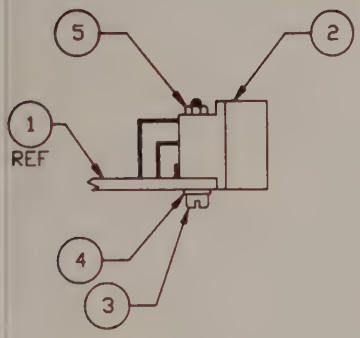


NOTES:

1. FOR GENERAL MANUFACTURING AND ENGINEERING NOTES SEE DWG. NO. A)401-0010.
2. THE MAXIMUM COMPONENT PROFILE IS .450

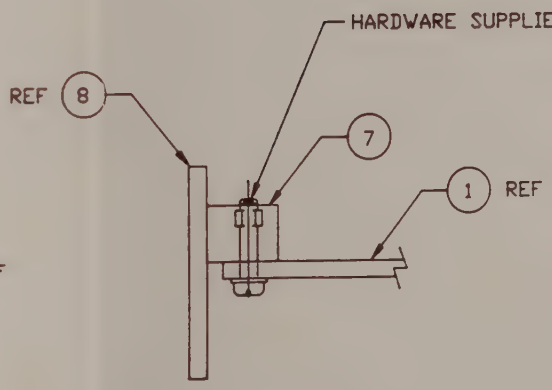
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	[-]	RELEASED	12/20/90	D.SEREMY
	A	REVISED PER ECO 21138	012591	T. KESLICKY





DETAIL A

SCALE 2:1



DETAIL B

SCALE 2:1

MARK DASH NUMBER, CURRENT REVISION AND SERIAL NO. PER MARKING SPEC 289-8004.

FOR PARTS LIST SEE PL 460-2255-501

DRAWN	K&H W.T.WARD	DATE 28NOV90	AYDIN COMPUTER AND MONITOR DIVISION, 700 DRESHER ROAD • HORSHAM, PA • 19044
CHECKED W.WARD		18DEC90	
DRAFTING W.WARD		18DEC90	CARD ASSEMBLY CPI012-1
ENGINEER J.WASIEWICZ		12/20/90	
MFG V.POLSKY		12/20/90	
APPROVED QA R.MULLER		12/20/90	SIZE D · CAGE CODE 20747 · AD460-2255-501 · REV A

	6197-4004
NEXT ASSY	USED ON

SHEET 1

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
—	RELEASED	12-20-90	D Jerrard
A	REV PER ECO 21138	022591	T. KESSLER

		CONTRACT NO.	AYDIN COMPUTER AND MONITOR Division 700 DRESHER ROAD HORSHAM. PA 19044
		DRAWN L. Wowk DATE 11/29/90	PARTS LIST CARD ASSEMBLY CPI012
		CHECKED W.T. Ward 3DEC90	
		DRAFTING W.T. Ward 3DEC90	
		APPROVED ENG J. MASIEWICZ 12/12/90	
	6197	APPROVED MFG V. Polak 12-20-90	SIZE A / CAGE CODE 20747 / DWG NO PL460-2255-501 / REV A
XT ASSY	USED ON	APPROVED QA 12-13-90	
APPLICATION			SCALE NONE / SHEET 1 of 3

00-0018E

PARTS LIST	DESIGN ACTIVITY IDENTIFICATION AYDIN COMPUTER AND MONITOR DIVISION HORSHAM, PA. 19044	CONTRACT NO. 6197	CAGE CODE 20747	PL460-2255-501	REV A

LIST TITLE CPI012-1 CARD ASSY	SUBCONTRACT NO.		SHEET NO. 2

IND NO	QTY REQ	U/M	CAGE CODE	DOCUMENT NUMBER	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES
001	1	EA	20747	400-2255-001	400-2255-001	P.C.BOARD CPI012-1	
002	3	EA	81312	108-199-018	108457096002971	DIN 96P RA MLE .093BD	P1 P2 P3
003	6	EA	15526	127-141-031	85ST-M2.5X12	SCR MET PAN 2.5X12MM	
004	6	EA	96906	128-200-803	MS15795-803	WASHER FLAT RD NO.4	
005	6	EA	15526	129-026-004	934ST-M2.5X.045	NUT HEX METRIC 2.5MM	
007	1	EA	20747	177-0120-001	177-0120-001	MOD .58W EUROCRD PNL ASSY	
008	2	EA		117-400-903	173-12525-B	BRACKET FRNT PNL VME	
011	6	EA	56289	102-367-685	150D685X9035B2	CAP 6.8UF 35V 10%	C1-C6
012	1	EA	73138	100-100-111	898-1-R1K	RESNET 15BUSD 1.0K	R1
013	1	EA	01121	100-110-204	314E180/390	RESNET 14PIN DIP 180/390 TERM	R2
014	1	EA		100-038-221	CFF-50-2200-F	MTFLM 220 OHM.125W 5%	
015	1	EA	50364	139-198-794	SN74LS794N	IC TTL 20 PIN	U31
016	2	EA		135-337-175	DS1000M-175	DLY LNE STAP 175 8P	U35 U36
017	2	EA	61772	139-918-003	IDT7202SA50P	IC MEM 1KX9 BIT 28P	U8 U9
018	2	EA	01295	139-198-138	SN74LS138N	3-8 DEC/DEM 16P	U7 U14
019	3	EA	01295	139-198-244	SN74LS244N	OCTAL BUF NINV 20P	U4 U6 U30
020	1	EA	01295	139-198-245	SN74LS245N	OCTAL BUSTRCVRNINV20P	U32
021	8	EA	01295	139-198-474	SN74LS74AN	DUAL FF/PR/CLR 14P	U12 U22 U23 U24 U26 U27 U44 U47
022	3	EA	01295	139-198-404	SN74LS04N	HEX INVERTER 14P	U16 U38 U45
023	2	EA	01295	139-198-486	SN74LS86N	QUAD 2IN OR 14P	U3 U5
024	2	EA	01295	139-198-400	SN74LS00N	QUAD 2IN NAND 14P	U13 U17
026	1	EA	01295	139-198-410	SN74LS10N	3IN PNAND 14P	U46
027	2	EA	01295	139-198-373	SN74LS373N	OCTAL-D-LATCH 20P	U39 U49

RTS / LIST	DESIGN ACTIVITY IDENTIFICATION: AYDIN COMPUTER AND MONITOR DIVISION, HORSHAM, PA. 19044	CONTRACT NO. 6197	CAGE CODE 20747	PL460-2255-501	REV A

LIST TITLE	SUBCONTRACT NO.	SHEET NO.
CPI012-1 CARD ASSY		3

IND NO	QTY REQ	U/M	CAGE CODE	DOCUMENT NUMBER	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES
028	1	EA	01295	139-198-402	SN74LS02N	QUAD 2INPT POS NOR 14PIN	U48
029	1	EA	01295	139-198-408	SN74LS08N	QUAD 2IN PAND 14P	U42
030	2	EA	01295	139-198-427	SN74LS27N	3 INPT POS NOR 14PIN	U21 U25
031	1	EA	01295	139-198-151	SN74LS151N	1-8DSEL/MULTPLX 16P	U33
032	3	EA	01295	139-198-157	SN74LS157N	2-1DSEL/MUX MINV 16P	U20 U34 U37
033	8	EA	18324	139-598-244	N74F244N	IC BUF'R OCTL 20 PIN	U10 U11 U18 U19 U28 U29 U40 U41
034	1	EA	AMS20	107-252-005	K40-5S	SWITCH L/P DIP 5 POS	SW1
035	1	EA	34335	139-596-002	AM26LS31PC	QUAD DIF LINE RX 16P	U1
036	1	EA	01295	139-198-430	SN74LS30N	8 INPUT NAND 14 PIN	U2
037	1	EA	01295	139-198-164	SN74LS164N	8BIT PAR OS REG 14P	U15
038	1	EA	07263	139-598-404	74F04PC	HEX INVERTER 14 PIN	U43
040	15	EA		108-985-1320	CIC-320-SGT-02-S	SCKT DIP W/CAP 20PIN	
045	7	EA		108-985-1316	CIC-316-SGT-02-S	SCKT DIP W/CAP 16PIN	
050	23	EA		108-985-1314	USCAC-314TE	SCKT DIP W/CAP 14PIN	
055	1	EA	55322	108-935-003	ICO-316-SGT	SCKT DIP 16 PN .3CTR	
060	1	EA	55322	108-935-002	ICO-314-SGT	SCKT DIP 14 PN .3CTR	
065	2	EA	55322	108-935-001	ICO-308-SGT	SCKT DIP 8 PIN .3CTR	
070	2	EA	55322	108-935-008	ICO-628-SGT	SCKT DIP 28PN .6 CTR	
075	AR	FT	17217	113-114-305	MC30010FHC-195G	WIRE W/WRP 30 AWG GREEN	
076	AR	FT	03890	114-001-006	6031 26 09 11	TUBING TEF 26 AWG WHT	
				AD 460-2255-501		ASSEMBLY DRAWING - CARD ASSY CPI012	
				LD 500-0988		LOGIC DIAGRAM - LOG DIA CPI012-1	

CPI012.S00	CPI012.S01
COVER SHT	P1 CONN

CPI012.S04	CPI012.S05
ADDRESS DECODE & READ/WRITE STROBES	CPI SETUP REGISTERS

CPI012.S08	CPI012.S09
DRB32-W FIFO OUTPUT & ATTENTION	DRB32-W INPUT CONTROL SIGNALS

SHEET	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
REV.															
SHEET	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45
REV.															
SHEET	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
REV.															
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
REV.	[-]	[-]	[-]	[-]	[-]	[-]	[-]	[-]	[-]	[-]	[-]				

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	—	RELEASED	4-11-91	

CPI012.S02
P2 CONN

CPI012.S03
P3 CONN

CPI012.S06
DAB32-W
FIFO
TRANSFER
ENABLE

CPI012.S07
DAB32-W
FIFO
WRITE\READ
CONTROL

CPI012.S10
DAB32-W
CH.#1
OUTPUTS

CPI012.S11
DAB32-W
CH.#2
OUTPUTS

60-2255-501	6197-5001
NEXT ASSY	USED ON
APPLICATION	

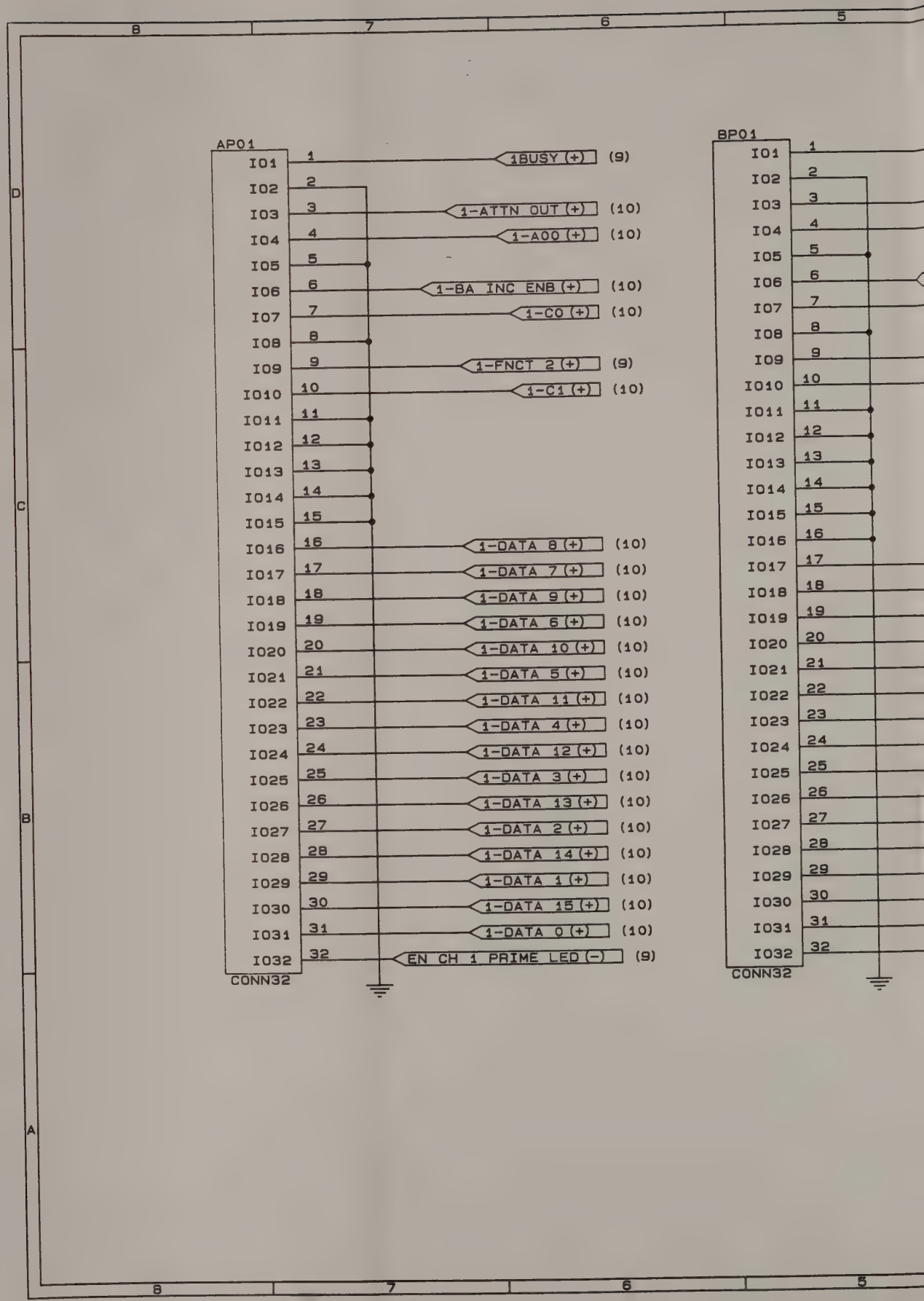
DRAWN M.ZARO	DATE 8/28/90
CHECKED W.Ward	11APR91
DRAFTING W.Ward	11APR91
ENGINEER ED HOLTZ	8/27/90
APPROVED Dan Sirent	4-11-91
MAGNETIC MEDIA	

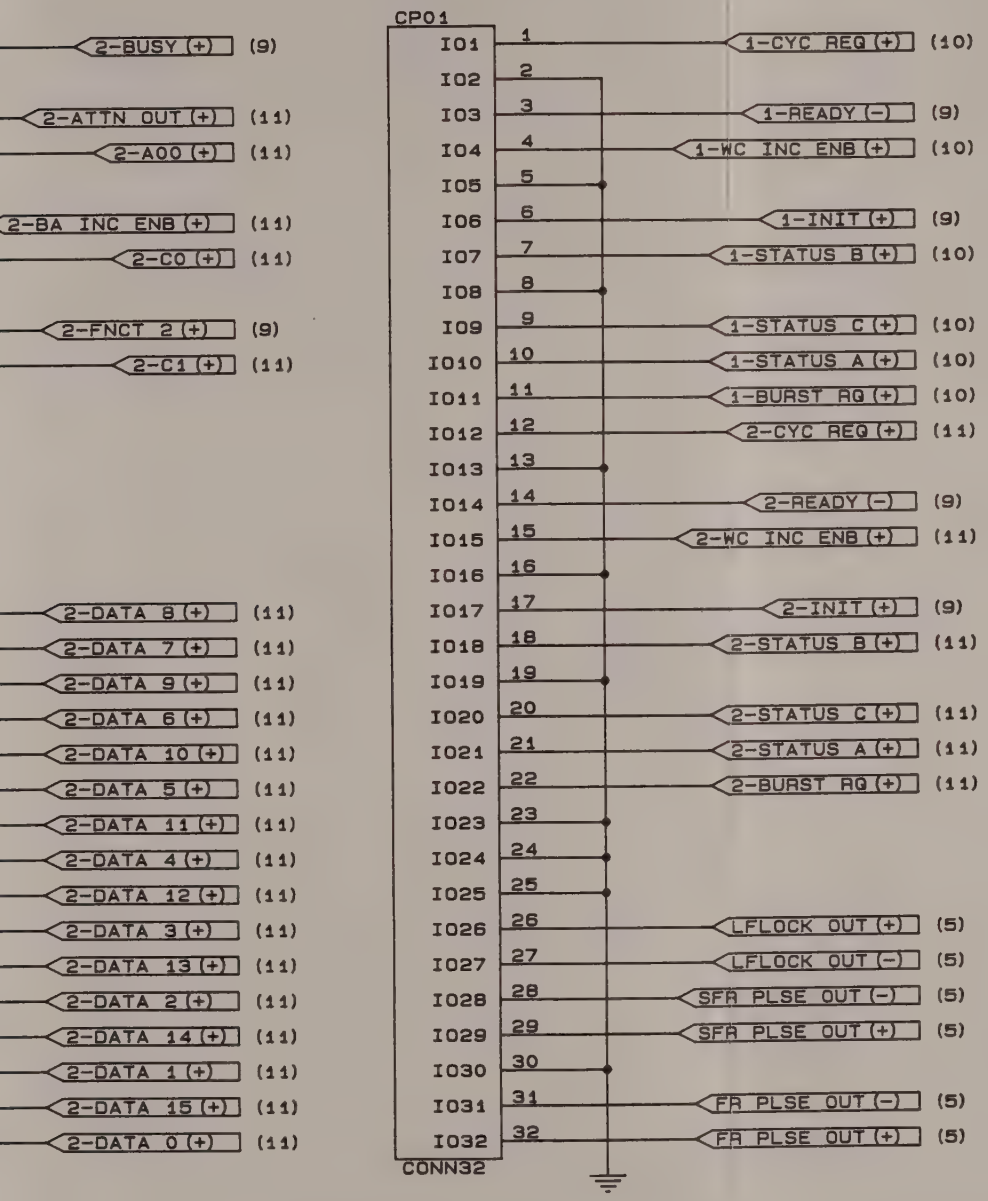
AYDIN COMPUTER AND MONITOR DIVISION
700 DRESHER ROAD
HORSHAM, PA. 19044

LOGIC DIAGRAM
CPI012

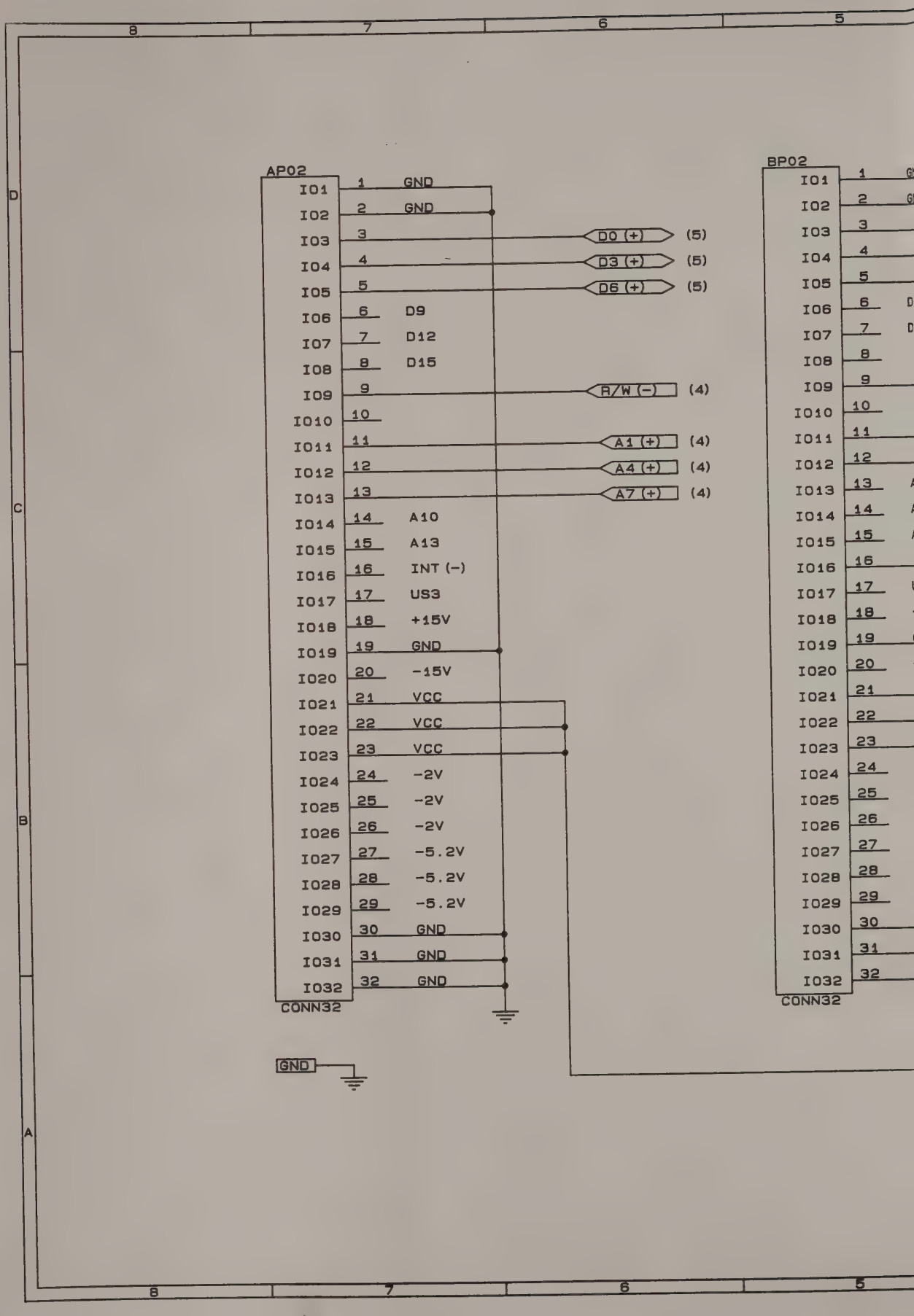
SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	20747	LD500-0988	[—]

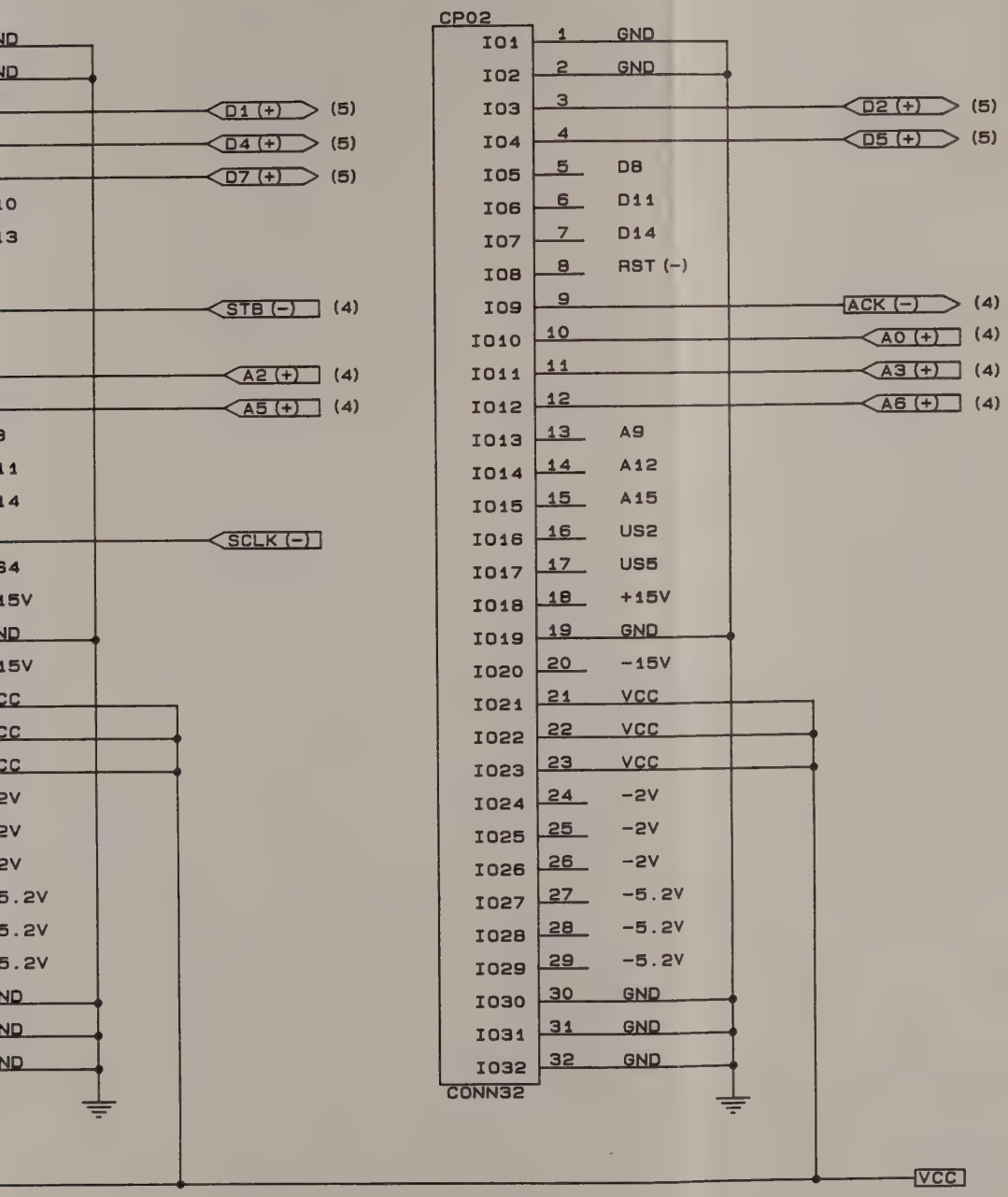
SHEET NO. 00 OF 11


8
7
6
5
D
C
B
A
AP01
IO01 1
IO02 2
IO03 3
IO04 4
IO05 5
IO06 6
IO07 7
IO08 8
IO09 9
IO010 10
IO011 11
IO012 12
IO013 13
IO014 14
IO015 15
IO016 16
IO017 17
IO018 18
IO019 19
IO020 20
IO021 21
IO022 22
IO023 23
IO024 24
IO025 25
IO026 26
IO027 27
IO028 28
IO029 29
IO030 30
IO031 31
IO032 32
CONN32
1BUSY (+) (9)
1-ATTN OUT (+) (10)
1-A00 (+) (10)
1-BA INC ENB (+) (10)
1-C0 (+) (10)
1-FNCT 2 (+) (9)
1-C1 (+) (10)
1-DATA 8 (+) (10)
1-DATA 7 (+) (10)
1-DATA 9 (+) (10)
1-DATA 6 (+) (10)
1-DATA 10 (+) (10)
1-DATA 5 (+) (10)
1-DATA 11 (+) (10)
1-DATA 4 (+) (10)
1-DATA 12 (+) (10)
1-DATA 3 (+) (10)
1-DATA 13 (+) (10)
1-DATA 2 (+) (10)
1-DATA 14 (+) (10)
1-DATA 1 (+) (10)
1-DATA 15 (+) (10)
1-DATA 0 (+) (10)
EN CH 1 PRIME LED (-) (9)
BP01
IO01 1
IO02 2
IO03 3
IO04 4
IO05 5
IO06 6
IO07 7
IO08 8
IO09 9
IO010 10
IO011 11
IO012 12
IO013 13
IO014 14
IO015 15
IO016 16
IO017 17
IO018 18
IO019 19
IO020 20
IO021 21
IO022 22
IO023 23
IO024 24
IO025 25
IO026 26
IO027 27
IO028 28
IO029 29
IO030 30
IO031 31
IO032 32
CONN32

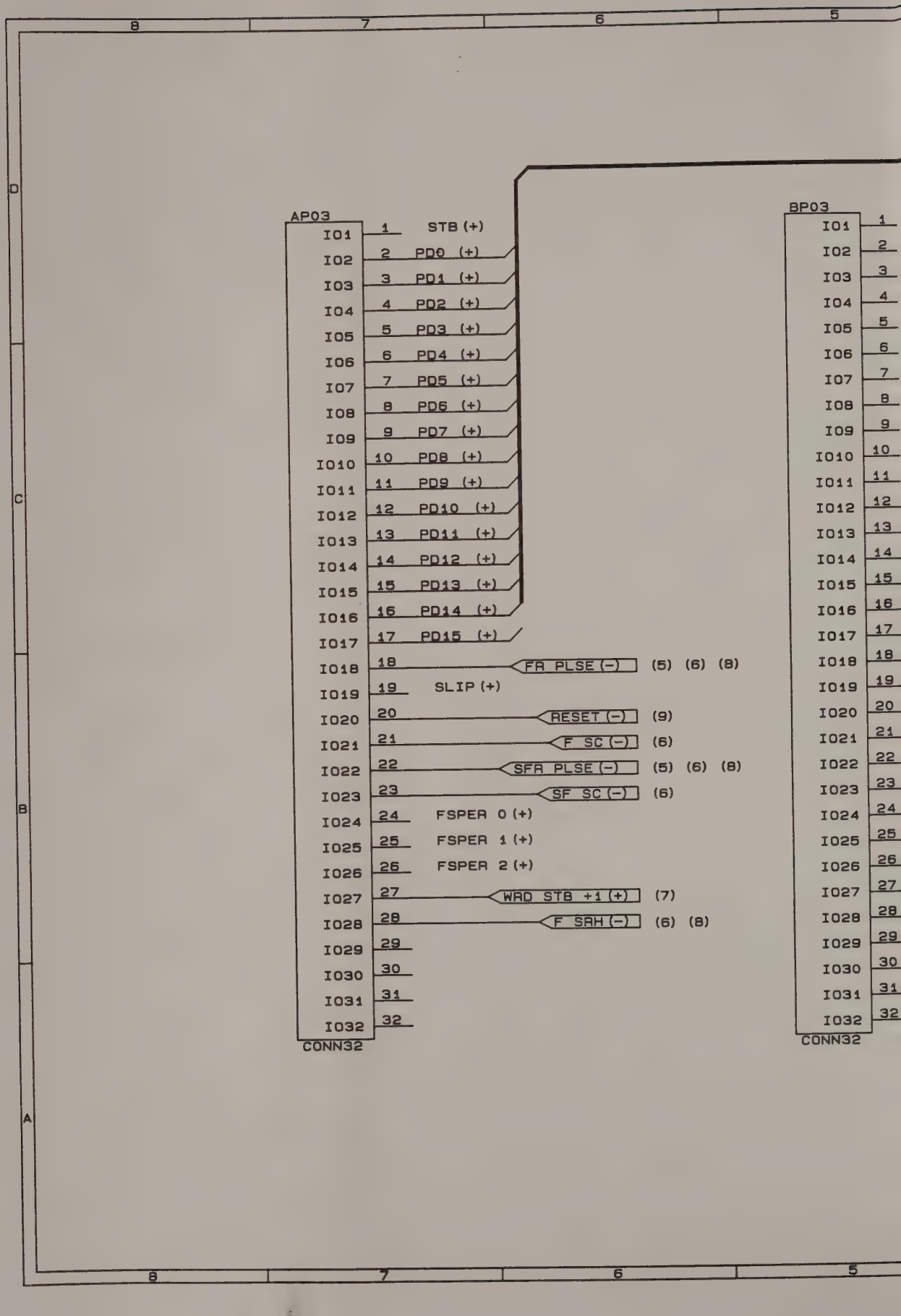


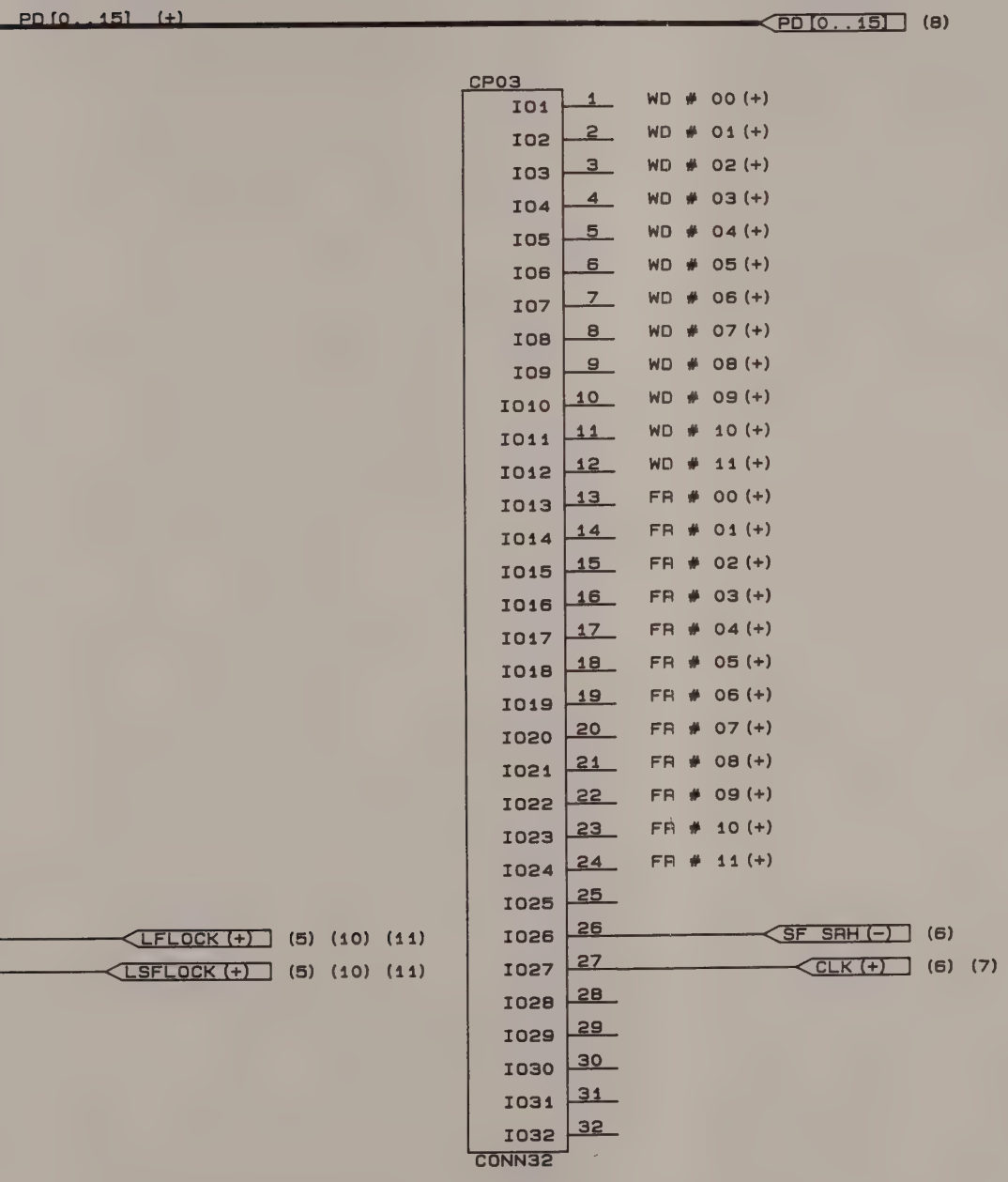
DRB32-W INTERFACES P1 CONNECTOR			
SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	20747	LD500-0988	[-]
		SHEET NO. 1 OF 1	


8
7
6
5
D
C
B
A
AP02
IO1 1 GND
IO2 2 GND
IO3 3
IO4 4
IO5 5
IO6 6 D9
IO7 7 D12
IO8 8 D15
IO9 9
IO10 10
IO11 11
IO12 12
IO13 13
IO14 14 A10
IO15 15 A13
IO16 16 INT (-)
IO17 17 US3
IO18 18 +15V
IO19 19 GND
IO20 20 -15V
IO21 21 VCC
IO22 22 VCC
IO23 23 VCC
IO24 24 -2V
IO25 25 -2V
IO26 26 -2V
IO27 27 -5.2V
IO28 28 -5.2V
IO29 29 -5.2V
IO30 30 GND
IO31 31 GND
IO32 32 GND
CONN32
D0 (+) (5)
D3 (+) (5)
D6 (+) (5)
R/W (-) (4)
A1 (+) (4)
A4 (+) (4)
A7 (+) (4)
GND
BP02
IO1 1
IO2 2
IO3 3
IO4 4
IO5 5
IO6 6
IO7 7
IO8 8
IO9 9
IO10 10
IO11 11
IO12 12
IO13 13
IO14 14
IO15 15
IO16 16
IO17 17
IO18 18
IO19 19
IO20 20
IO21 21
IO22 22
IO23 23
IO24 24
IO25 25
IO26 26
IO27 27
IO28 28
IO29 29
IO30 30
IO31 31
IO32 32
CONN32

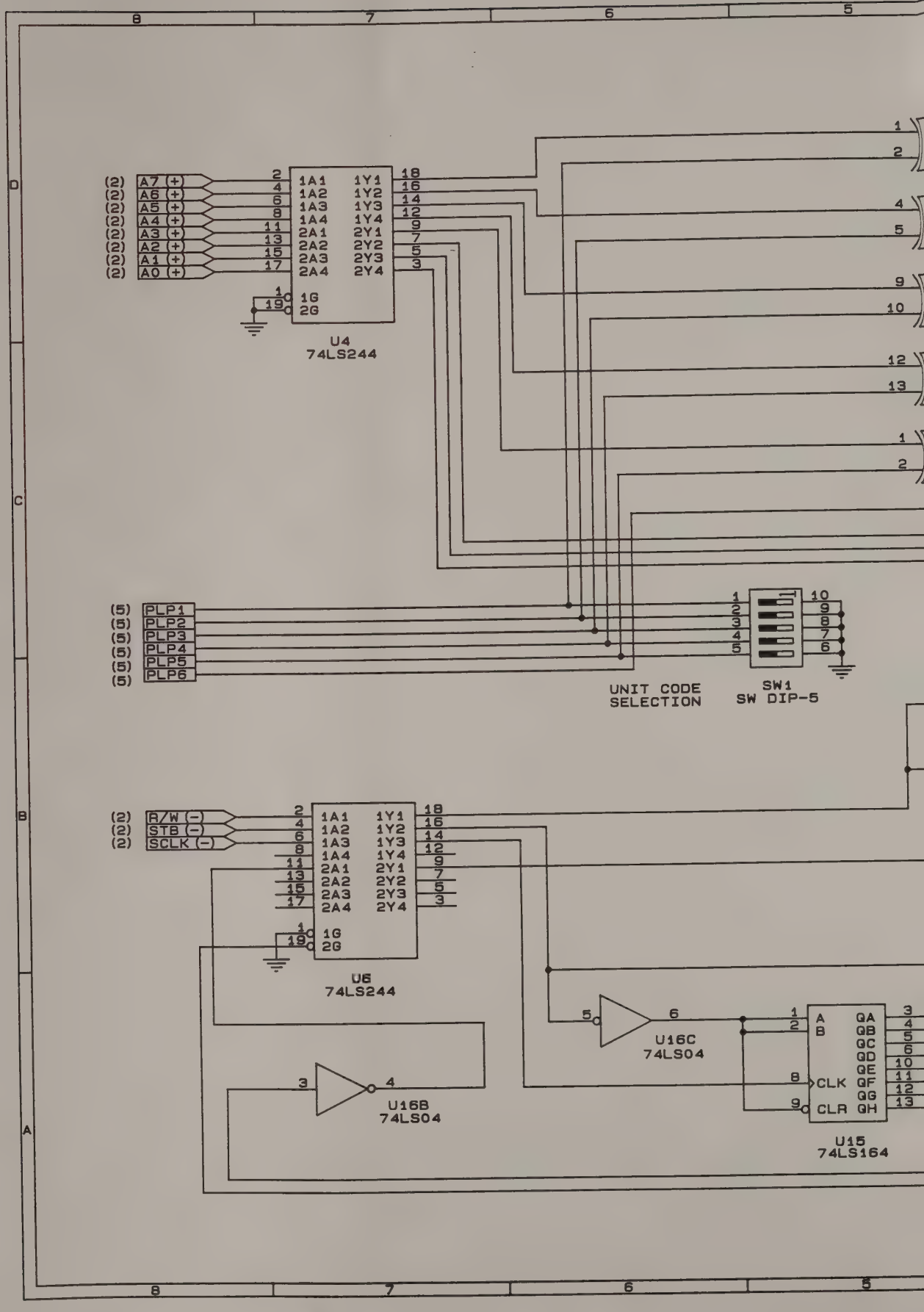


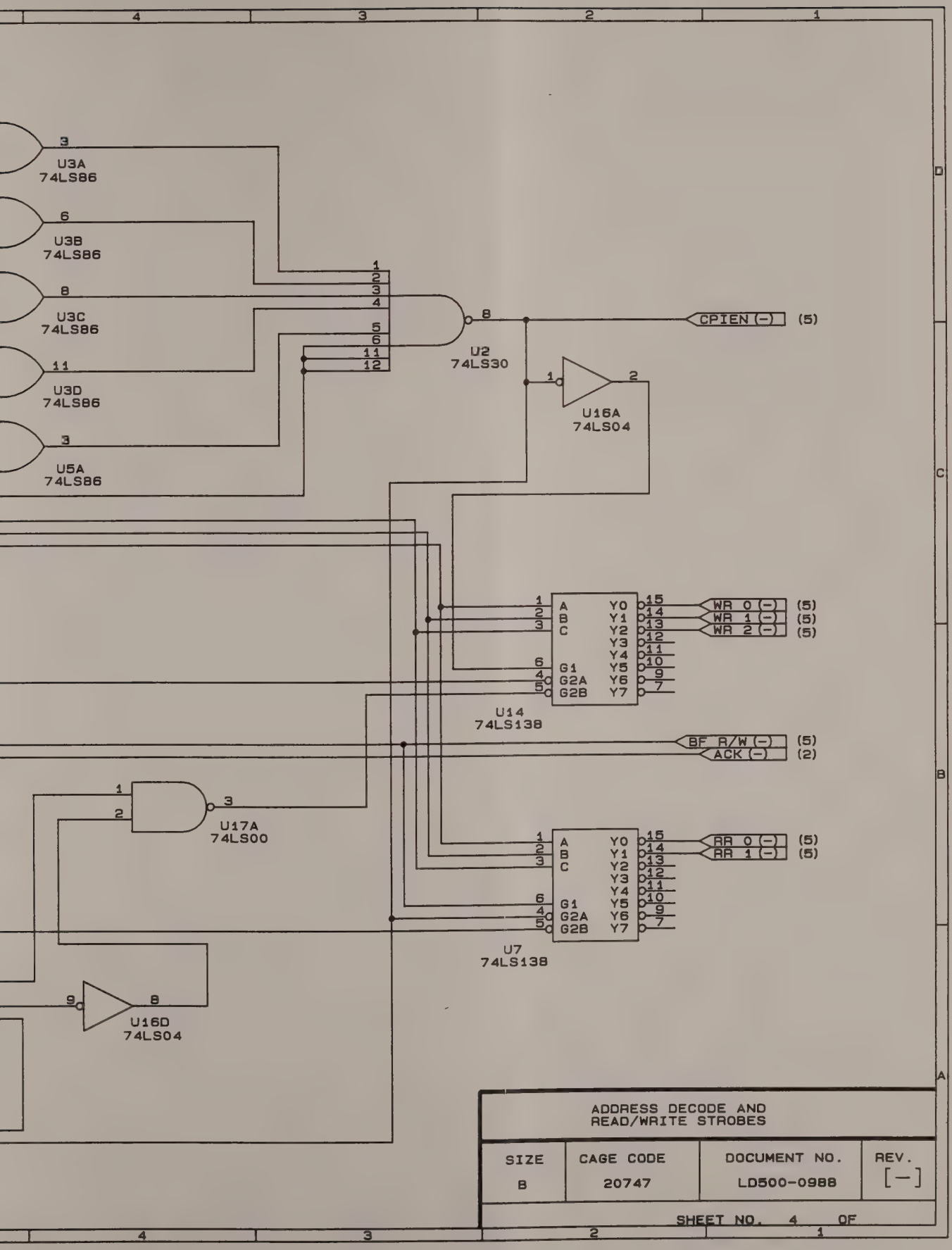
IOC BUS POWER P2 CONNECTOR			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0988	REV. [-]
SHEET NO. 2 OF			


8
7
6
5
D
C
B
A
AP03
IO1 1 STB (+)
IO2 2 PD0 (+)
IO3 3 PD1 (+)
IO4 4 PD2 (+)
IO5 5 PD3 (+)
IO6 6 PD4 (+)
IO7 7 PD5 (+)
IO8 8 PD6 (+)
IO9 9 PD7 (+)
IO10 10 PD8 (+)
IO11 11 PD9 (+)
IO12 12 PD10 (+)
IO13 13 PD11 (+)
IO14 14 PD12 (+)
IO15 15 PD13 (+)
IO16 16 PD14 (+)
IO17 17 PD15 (+)
IO18 18 FR PLSE (-) (5) (6) (8)
IO19 19 SLIP (+)
IO20 20 RESET (-) (9)
IO21 21 F SC (-) (6)
IO22 22 SFR PLSE (-) (5) (6) (8)
IO23 23 SF SC (-) (6)
IO24 24 FSPER 0 (+)
IO25 25 FSPER 1 (+)
IO26 26 FSPER 2 (+)
IO27 27 WRD STB +1 (+) (7)
IO28 28 F SAH (-) (6) (8)
IO29 29
IO30 30
IO31 31
IO32 32
CONN32
BP03
IO1 1
IO2 2
IO3 3
IO4 4
IO5 5
IO6 6
IO7 7
IO8 8
IO9 9
IO10 10
IO11 11
IO12 12
IO13 13
IO14 14
IO15 15
IO16 16
IO17 17
IO18 18
IO19 19
IO20 20
IO21 21
IO22 22
IO23 23
IO24 24
IO25 25
IO26 26
IO27 27
IO28 28
IO29 29
IO30 30
IO31 31
IO32 32
CONN32

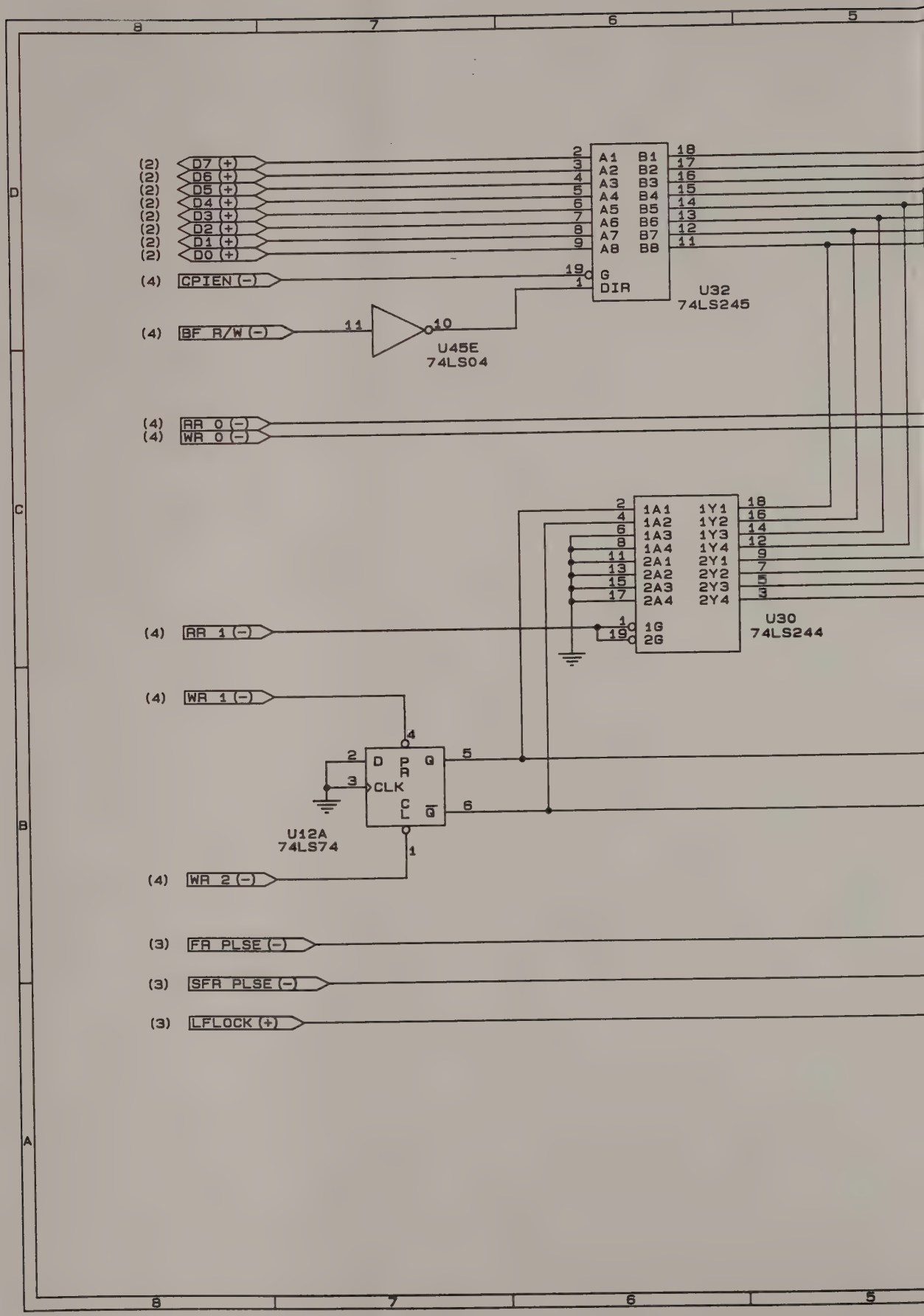


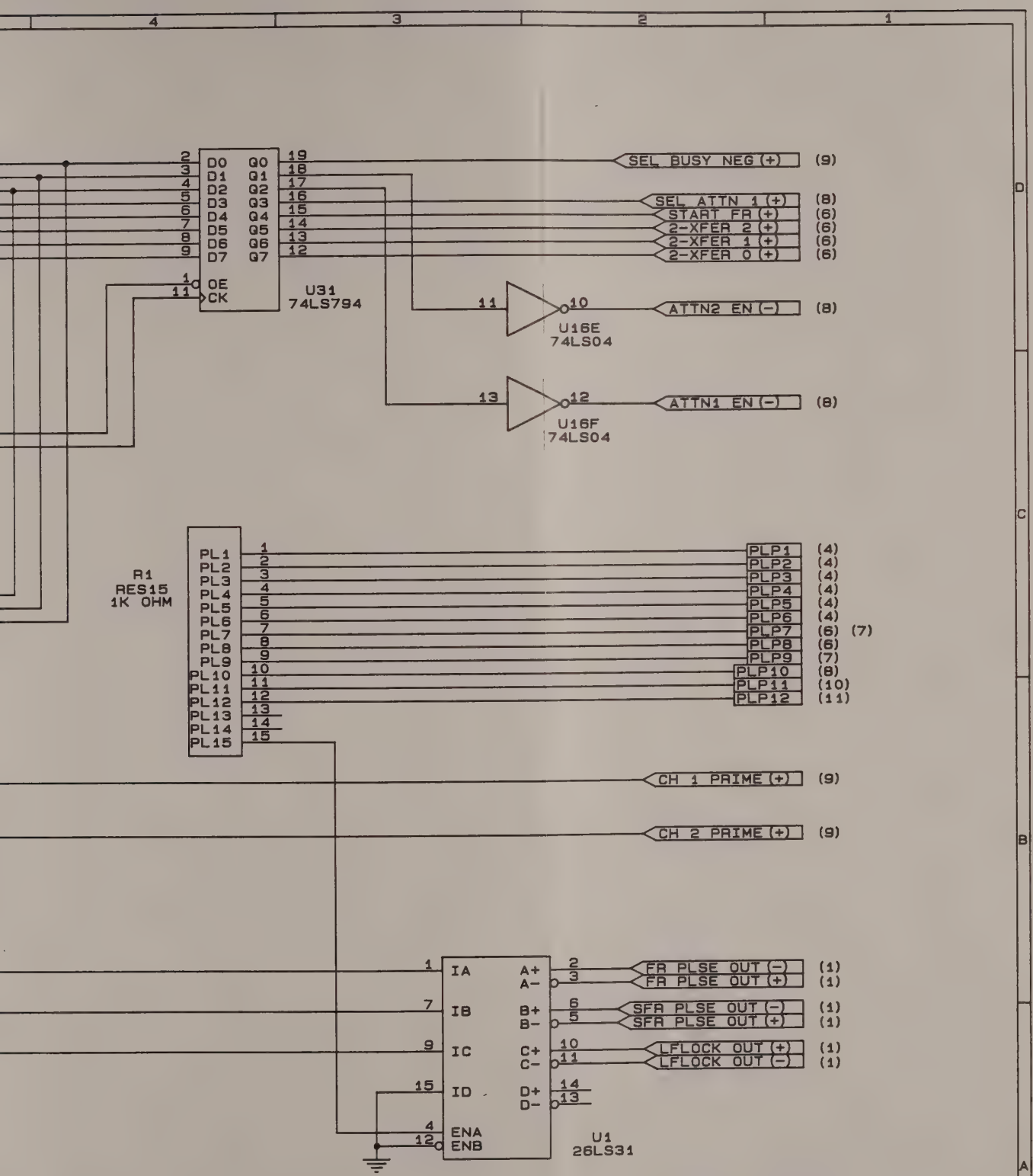
FRAME SYNC INTERFACE P3 CONNECTOR			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0988	REV. [-]
SHEET NO. 3 OF			


8
7
6
5
D
C
B
A
(2) A7 (+)
(2) A6 (+)
(2) A5 (+)
(2) A4 (+)
(2) A3 (+)
(2) A2 (+)
(2) A1 (+)
(2) A0 (+)
1A1 1Y1
1A2 1Y2
1A3 1Y3
1A4 1Y4
2A1 2Y1
2A2 2Y2
2A3 2Y3
2A4 2Y4
1G
2G
U4
74LS244
(5) PLP1
(5) PLP2
(5) PLP3
(5) PLP4
(5) PLP5
(5) PLP6
UNIT CODE
SELECTION
SW1
SW DIP-5
(2) R/W (-)
(2) STB (-)
(2) SCLK (-)
U6
74LS244
U16C
74LS04
U16B
74LS04
A
B
CLK
CLR
QA
QB
QC
QD
QE
QF
QG
QH
U15
74LS164

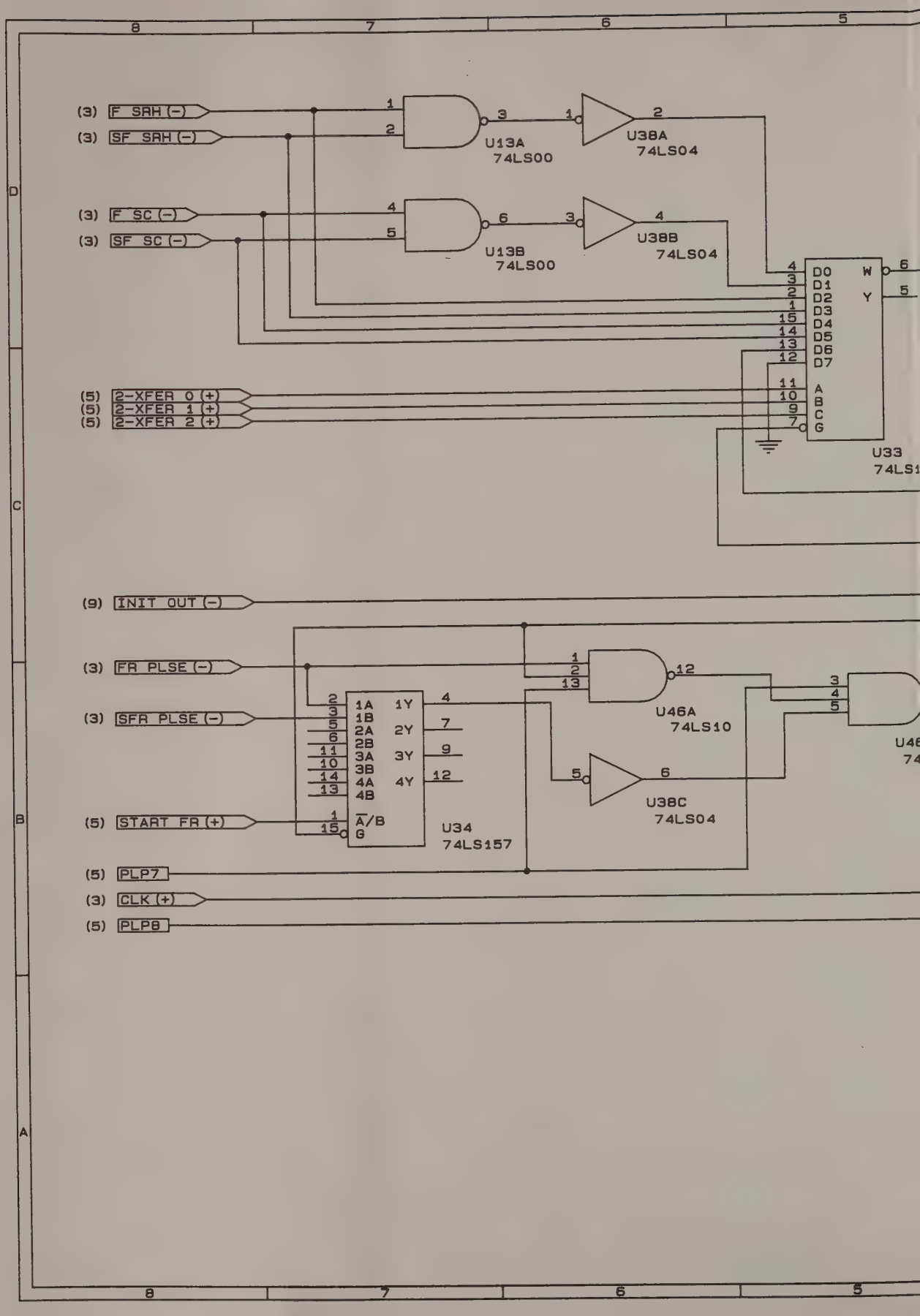


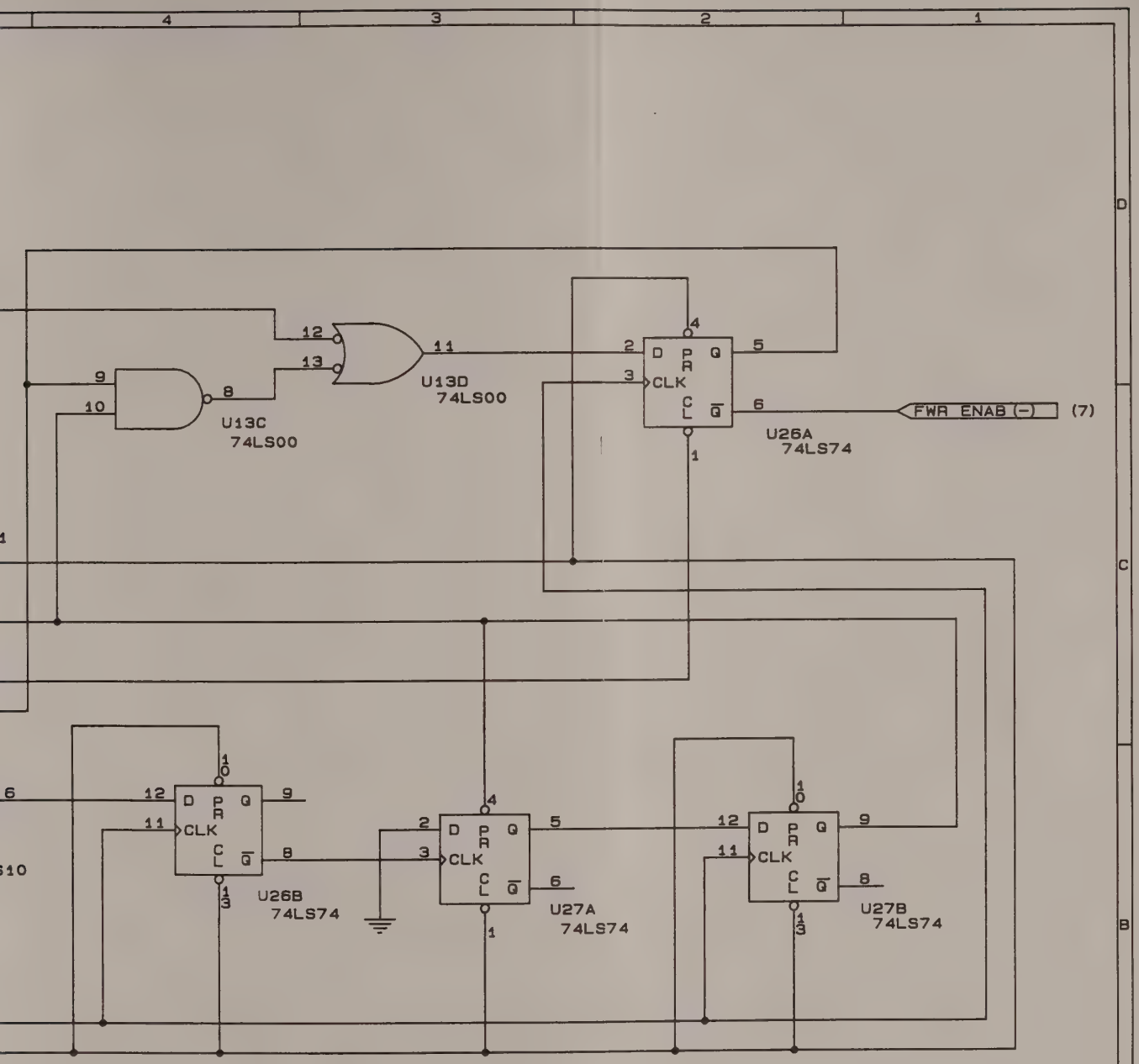
ADDRESS DECODE AND READ/WRITE STROBES			
SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	20747	LD500-0988	[-]
SHEET NO. 4 OF			


8
7
6
5
D
C
B
A
(2) D7 (+)
(2) D6 (+)
(2) D5 (+)
(2) D4 (+)
(2) D3 (+)
(2) D2 (+)
(2) D1 (+)
(2) D0 (+)
(4) CPIEN (-)
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
G
DIR
U32
74LS245
(4) BF R/W (-)
U45E
74LS04
(4) RR 0 (-)
(4) WR 0 (-)
1A1 1A2 1A3 1A4 2A1 2A2 2A3 2A4
1Y1 1Y2 1Y3 1Y4 2Y1 2Y2 2Y3 2Y4
1G
2G
U30
74LS244
(4) RR 1 (-)
(4) WR 1 (-)
D
CLK
PR
CLR
Q
U12A
74LS74
(4) WR 2 (-)
(3) FR PLSE (-)
(3) SFR PLSE (-)
(3) LFLOCK (+)

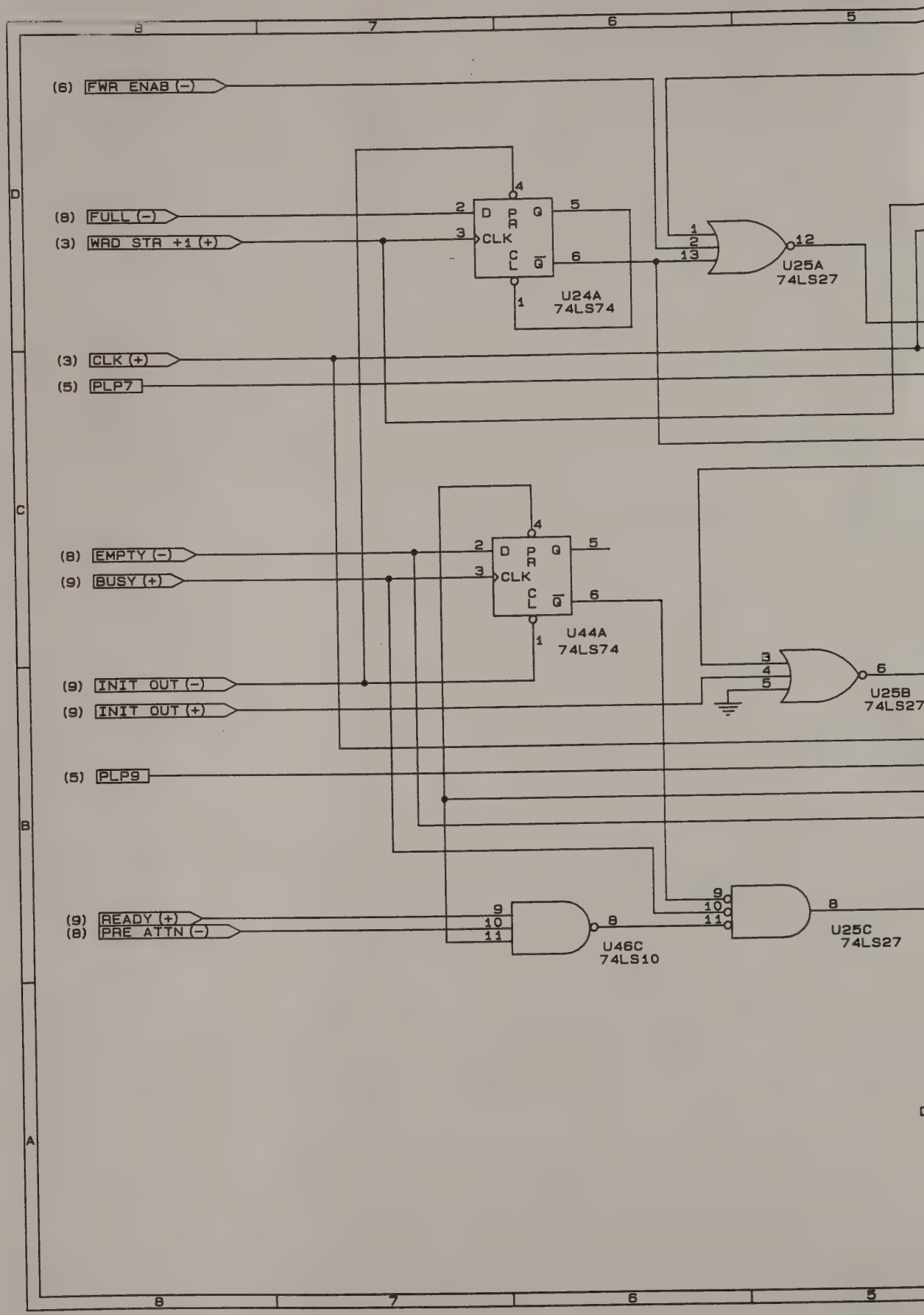


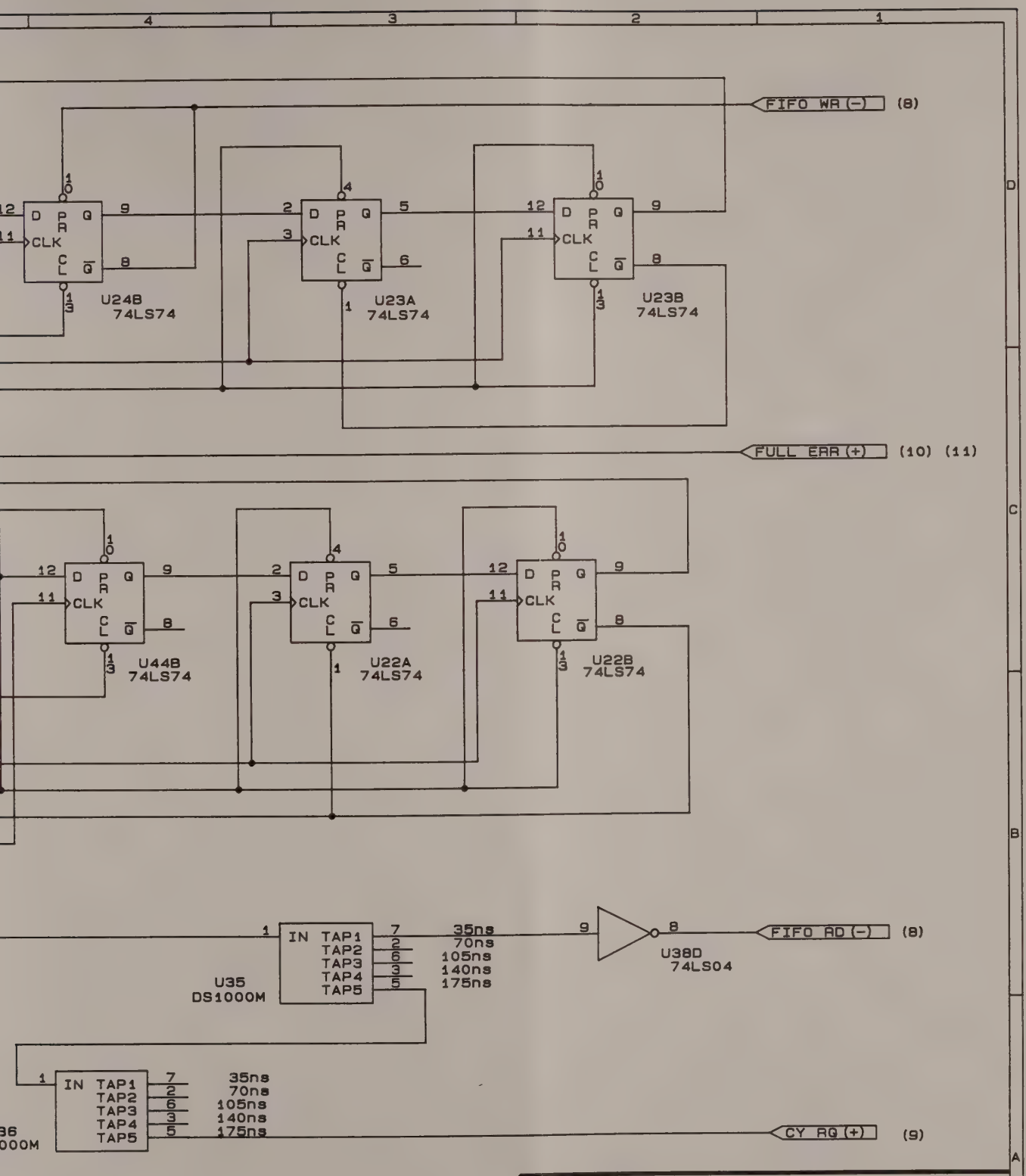
CPI SETUP REGISTERS & STATUS OUTPUTS			
SIZE	CAGE CODE	DOCUMENT NO.	REV.
B	20747	LD500-0988	[—]
		SHEET NO. 5 OF	


8
7
6
5
D
C
B
A
(3) F SRH (-)
(3) SF SRH (-)
U13A
74LS00
U38A
74LS04
(3) F SC (-)
(3) SF SC (-)
U13B
74LS00
U38B
74LS04
D0
D1
D2
D3
D4
D5
D6
D7
W
Y
A
B
C
G
U33
74LS1
(5) 2-XFER 0 (+)
(5) 2-XFER 1 (+)
(5) 2-XFER 2 (+)
(9) INIT OUT (-)
(3) FR PLSE (-)
(3) SFR PLSE (-)
1A
1B
2A
2B
3A
3B
4A
4B
1Y
2Y
3Y
4Y
U34
74LS157
U46A
74LS10
U38C
74LS04
U46
74
(5) START FR (+)
A/B
G
(5) PLP7
(3) CLK (+)
(5) PLP8

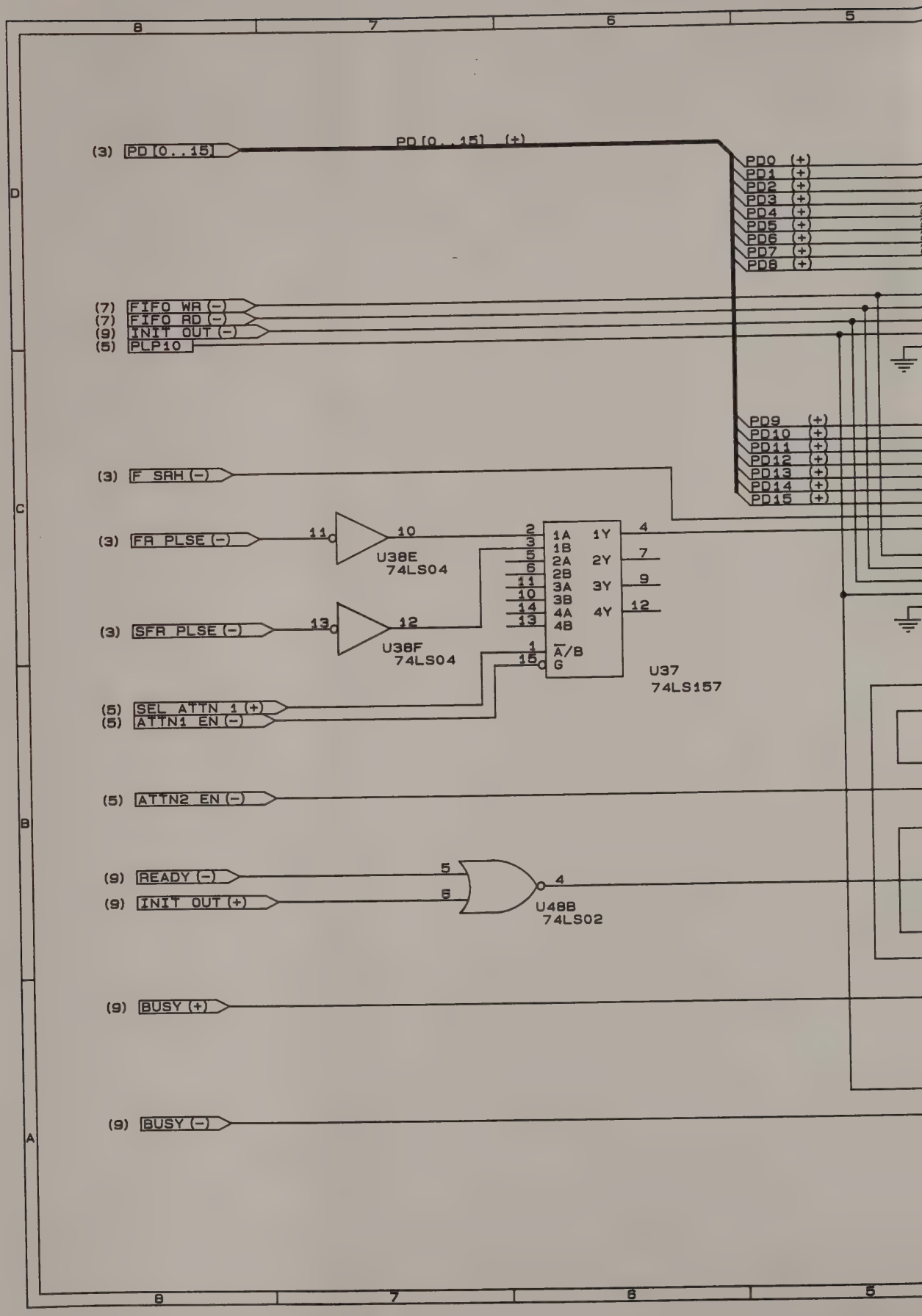


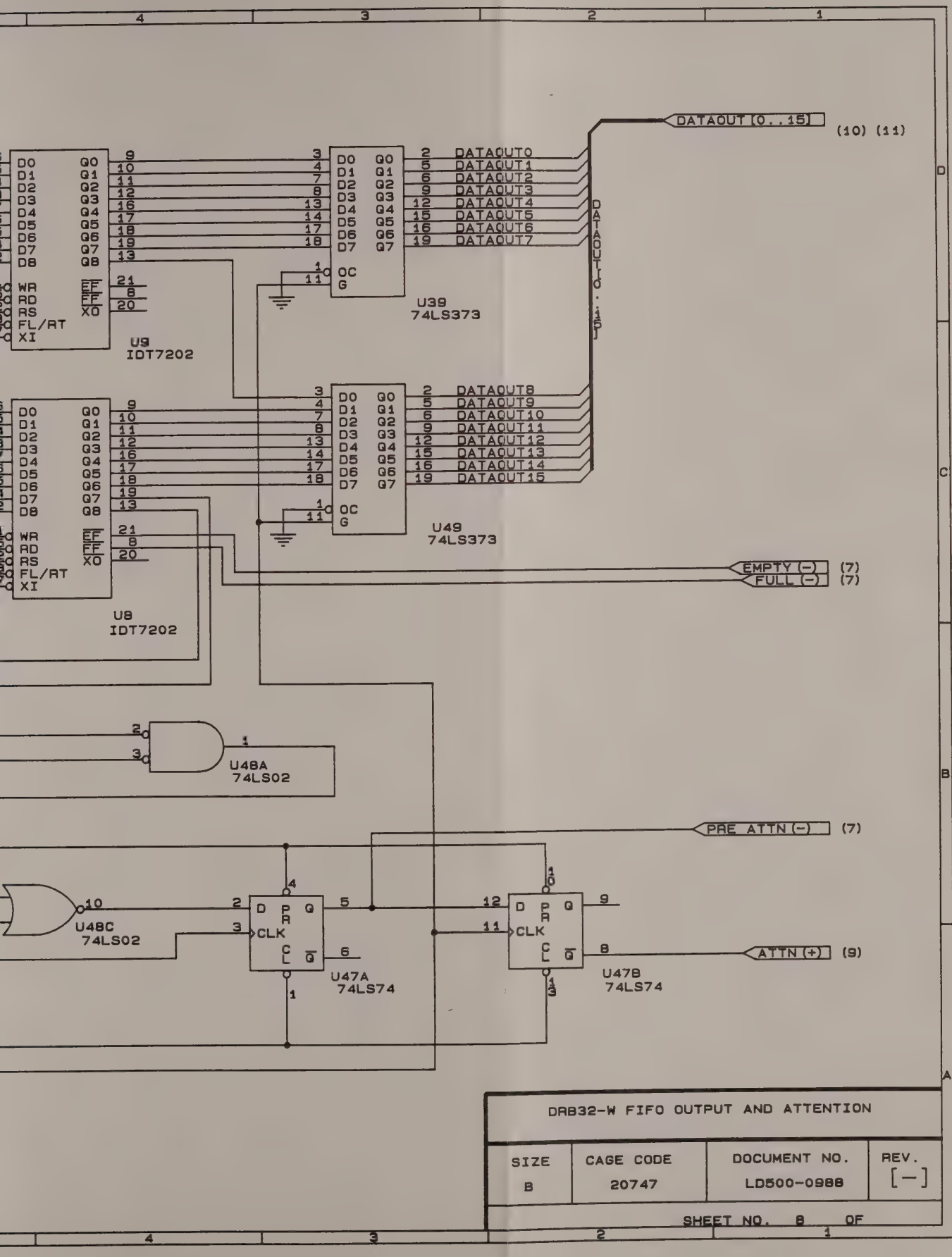
DRB32-W FIFO TRANSFER ENABLE			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0988	REV. [-]
		SHEET NO. 6 OF	


8
7
6
5
D
C
B
A
(6) FWR ENAB (-)
(8) FULL (-)
(3) WRD STR +1 (+)
(3) CLK (+)
(5) PLP7
(8) EMPTY (-)
(9) BUSY (+)
(9) INIT OUT (-)
(9) INIT OUT (+)
(5) PLP9
(9) READY (+)
(8) PRE ATTN (-)
U24A
74LS74
U25A
74LS27
U44A
74LS74
U25B
74LS27
U46C
74LS10
U25C
74LS27

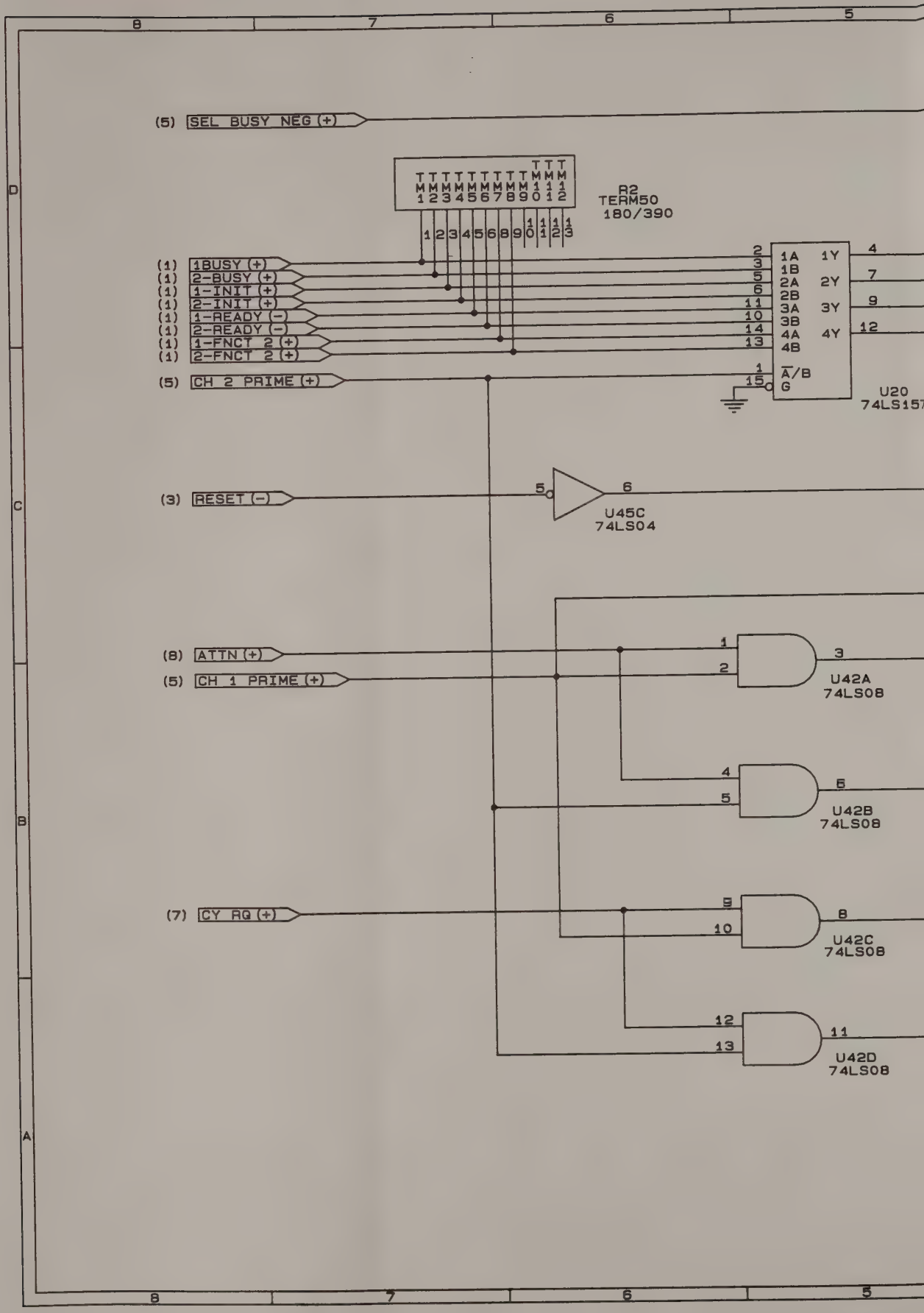


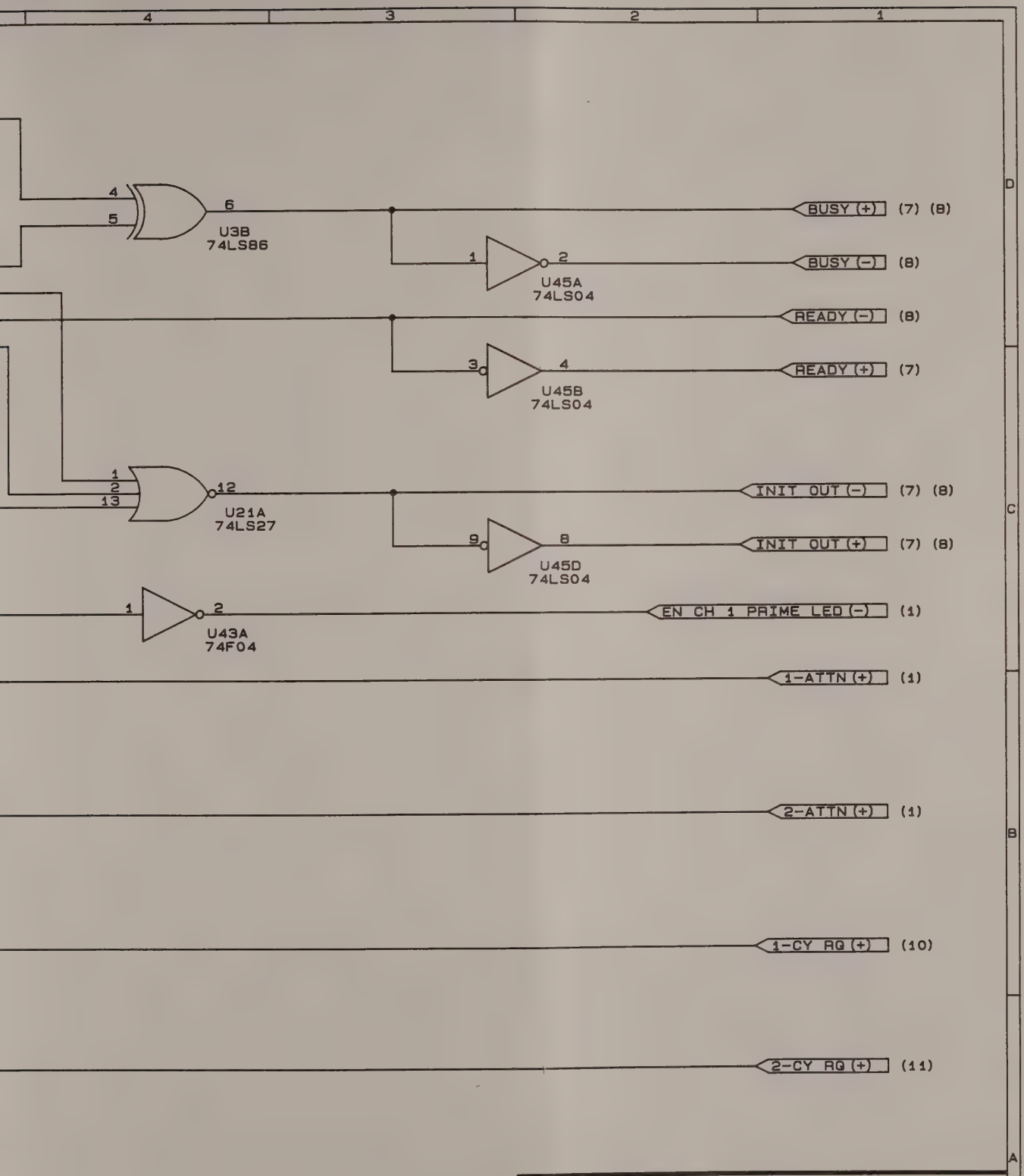
DRB32-W FIFO WRITE \ READ CONTROL			
SIZE B	CAGE CODWE 20747	DOCUMENT NO. LD500-0988	REV. [—]
SHEET NO. 7 OF			


8
7
6
5
D
C
B
A
(3) PD[0..15]
PD[0..15] (+)
PD0 (+)
PD1 (+)
PD2 (+)
PD3 (+)
PD4 (+)
PD5 (+)
PD6 (+)
PD7 (+)
PD8 (+)
(7) FIFO WR (-)
(7) FIFO RD (-)
(9) INIT OUT (-)
(5) PLP10
PD9 (+)
PD10 (+)
PD11 (+)
PD12 (+)
PD13 (+)
PD14 (+)
PD15 (+)
(3) F SAH (-)
(3) FR PLSE (-)
(3) SFR PLSE (-)
U38E
74LS04
U38F
74LS04
U37
74LS157
1A
1B
2A
2B
3A
3B
4A
4B
1Y
2Y
3Y
4Y
A/B
G
(5) SEL ATTN 1 (+)
(5) ATTN1 EN (-)
(5) ATTN2 EN (-)
(9) READY (-)
(9) INIT OUT (+)
U48B
74LS02
(9) BUSY (+)
(9) BUSY (-)

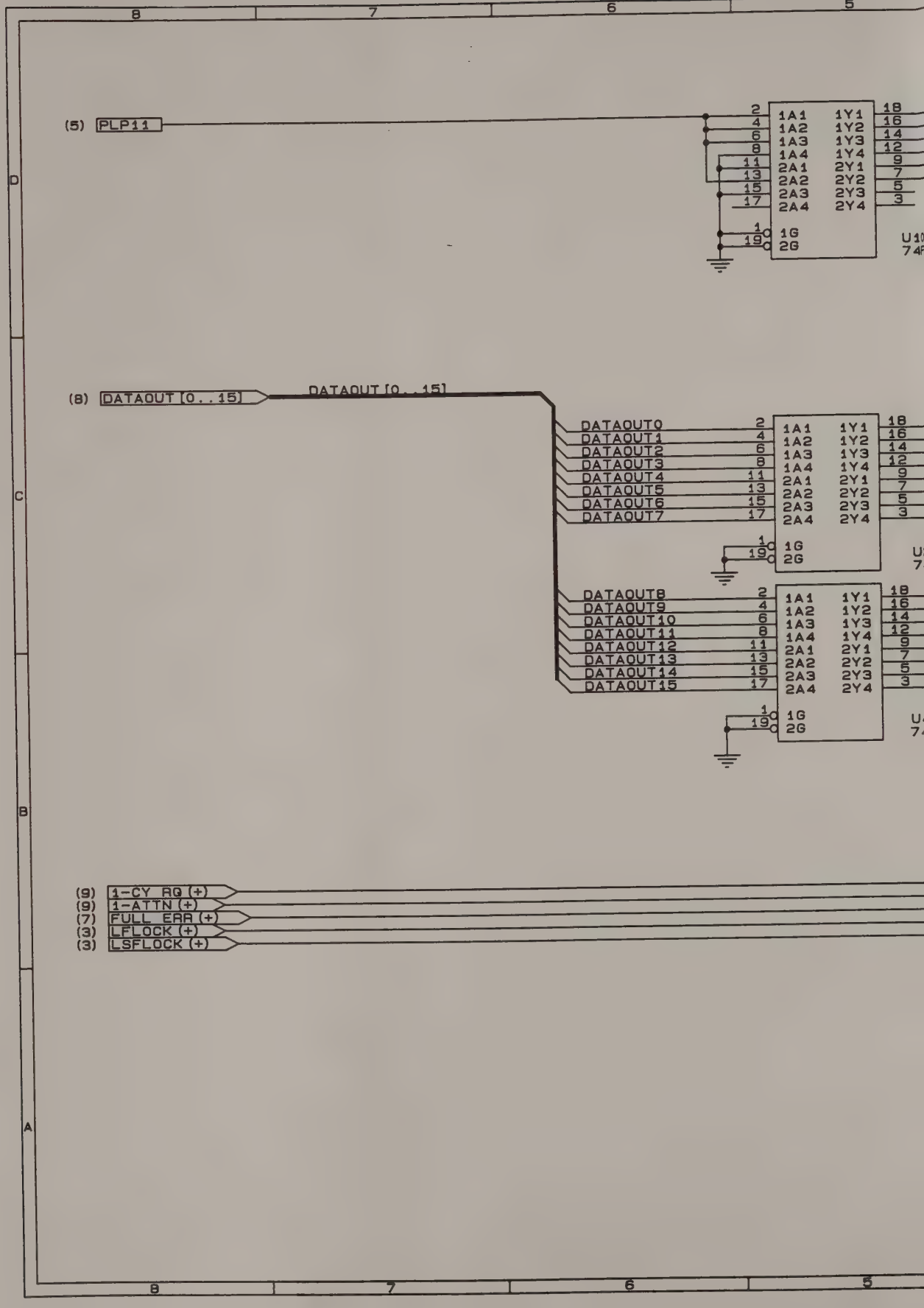


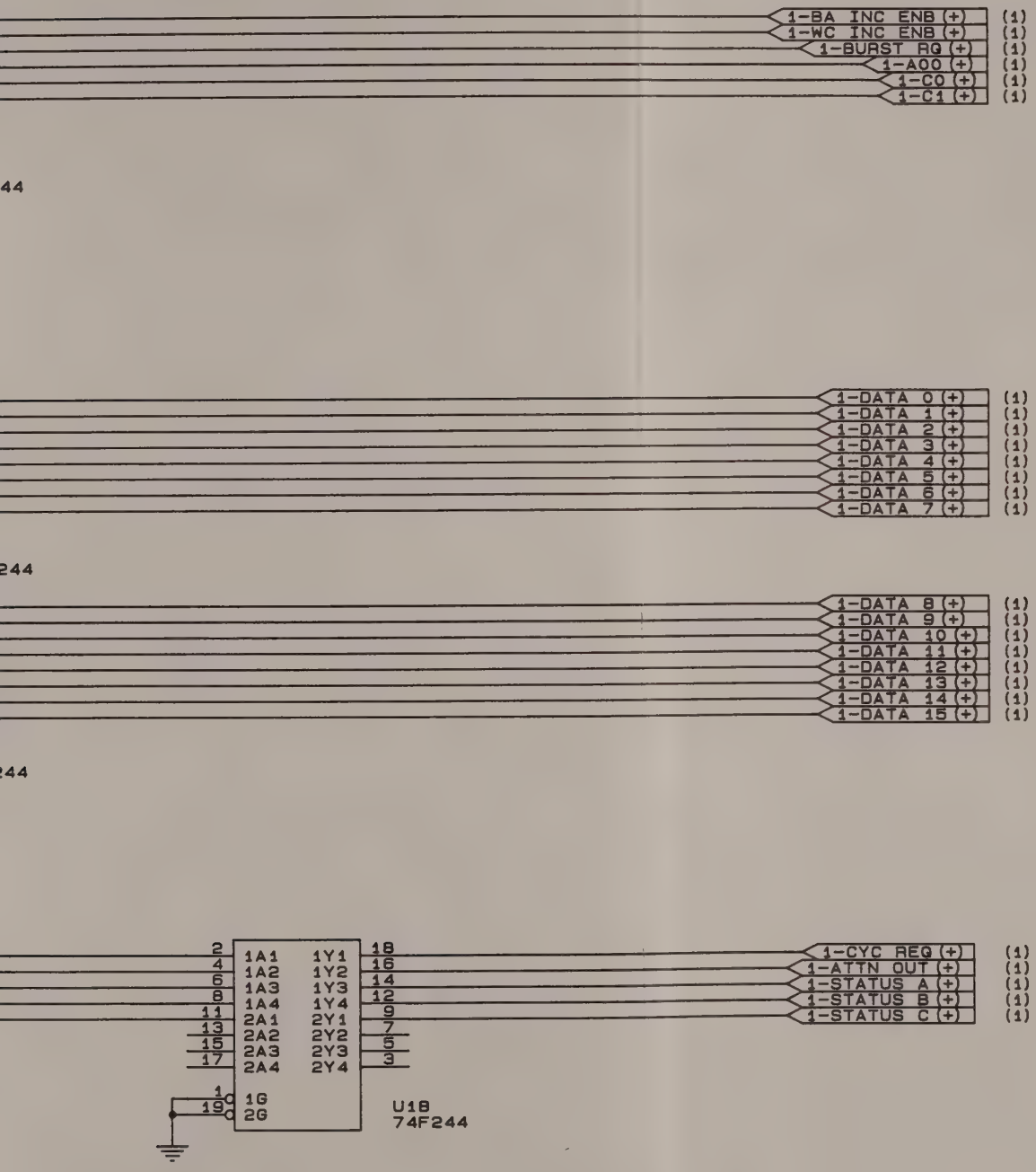
DRB32-W FIFO OUTPUT AND ATTENTION			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0988	REV. [-]
SHEET NO. 8 OF			


8
7
6
5
D
C
B
A
(5) SEL BUSY NEG (+)
TTMM 1234
TTTTTTTTTTTTTTMM 56789012
R2
TERM50
180/390
1 2 3 4 5 6 8 9 10 11 12 13
(1) 1BUSY (+)
(1) 2-BUSY (+)
(1) 1-INIT (+)
(1) 2-INIT (+)
(1) 1-READY (-)
(1) 2-READY (-)
(1) 1-FNCT 2 (+)
(1) 2-FNCT 2 (+)
(5) CH 2 PRIME (+)
2 3 5 6 11 10 14 13 1 15
1A 1B 2A 2B 3A 3B 4A 4B A/B G
1Y 2Y 3Y 4Y
4 7 9 12
U20
74LS157
(3) RESET (-)
5
6
U45C
74LS04
(8) ATTN (+)
(5) CH 1 PRIME (+)
1 2
3
U42A
74LS08
4 5
6
U42B
74LS08
(7) CY RQ (+)
9 10
8
U42C
74LS08
12 13
11
U42D
74LS08

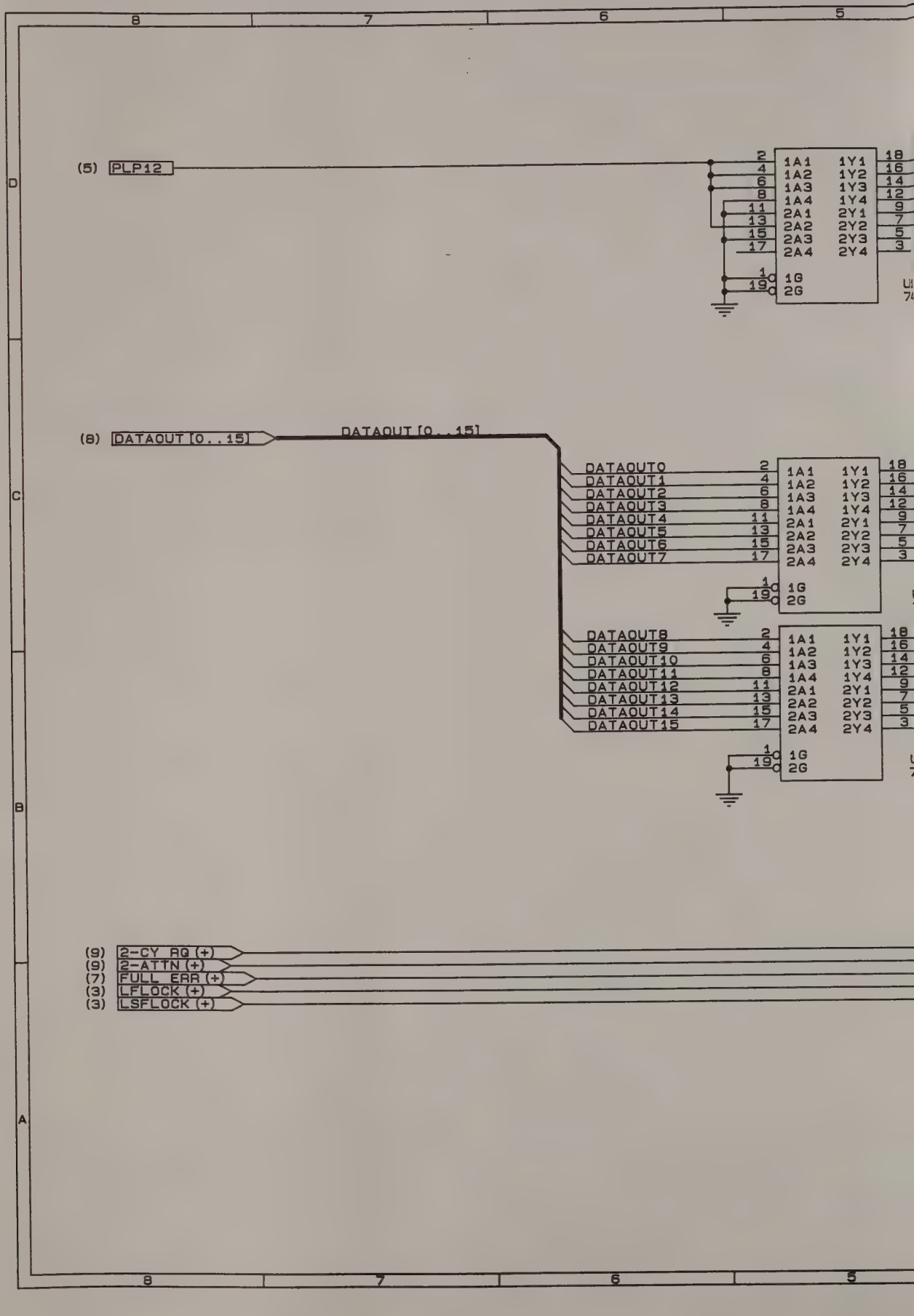


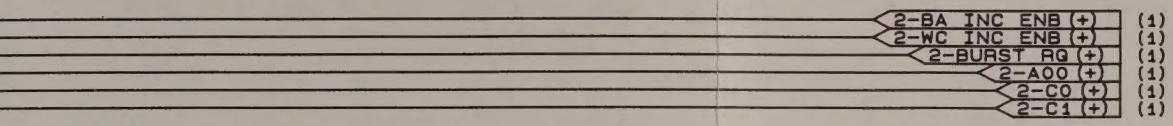
DRB32-W INPUT CONTROL SIGNALS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0988	REV. [—]
SHEET NO. 9 OF			


8
7
6
5
D
C
B
A
(5) PLP11
1A1
1A2
1A3
1A4
2A1
2A2
2A3
2A4
1G
2G
1Y1
1Y2
1Y3
1Y4
2Y1
2Y2
2Y3
2Y4
(8) DATAOUT[0..15]
DATAOUT[0..15]
DATAOUT0
DATAOUT1
DATAOUT2
DATAOUT3
DATAOUT4
DATAOUT5
DATAOUT6
DATAOUT7
DATAOUT8
DATAOUT9
DATAOUT10
DATAOUT11
DATAOUT12
DATAOUT13
DATAOUT14
DATAOUT15
(9) 1-CY RQ (+)
(9) 1-ATTN (+)
(7) FULL ERR (+)
(3) LFLOCK (+)
(3) LSFLOCK (+)

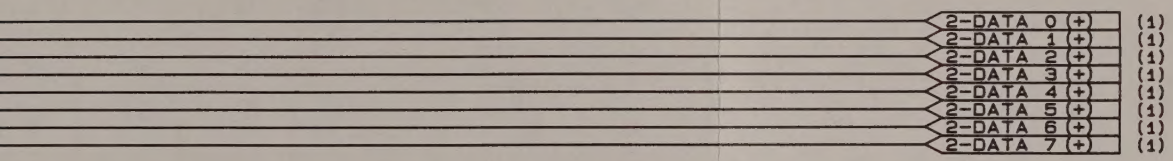


DRB32-W CH.#1 OUTPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0988	REV. [-]
SHEET NO. 10 OF			

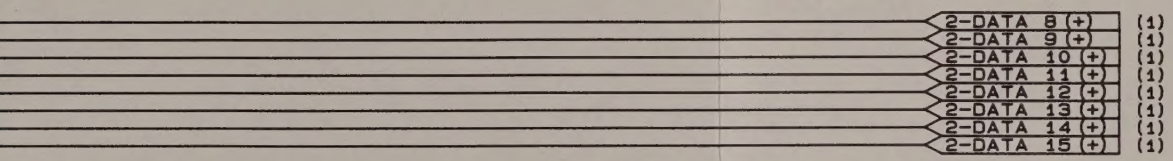

8
7
6
5
D
C
B
A
(5) PLP12
1A1
1A2
1A3
1A4
2A1
2A2
2A3
2A4
1G
2G
1Y1
1Y2
1Y3
1Y4
2Y1
2Y2
2Y3
2Y4
(8) DATAOUT[0..15]
DATAOUT[0..15]
DATAOUT0
DATAOUT1
DATAOUT2
DATAOUT3
DATAOUT4
DATAOUT5
DATAOUT6
DATAOUT7
DATAOUT8
DATAOUT9
DATAOUT10
DATAOUT11
DATAOUT12
DATAOUT13
DATAOUT14
DATAOUT15
(9) 2-CY RQ (+)
(9) 2-ATTN (+)
(7) FULL ERR (+)
(3) LFLOCK (+)
(3) LSFLOCK (+)



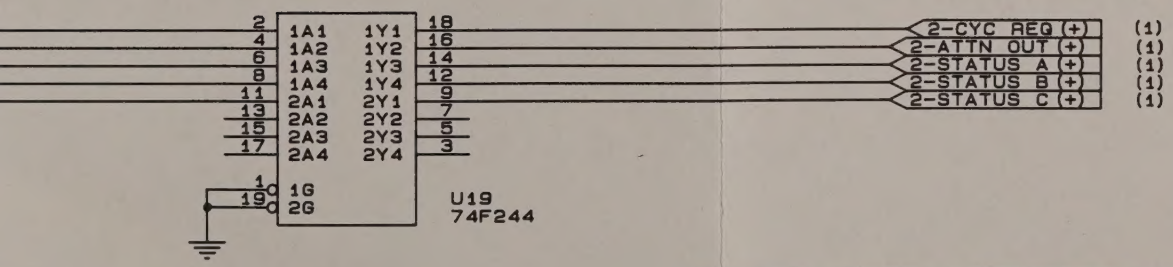
244



F244



F244



DRB32-W CH.#2 OUTPUTS			
SIZE B	CAGE CODE 20747	DOCUMENT NO. LD500-0988	REV. [—]
SHEET NO. 11 OF			